THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND

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THE VOYAGER (MJS)

LECP

PULSE HEIGHT ANALYZER

(PHA)

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THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL MARYLAND

PREFACE

The Applied Physics Laboratory S1P Group has an experiment to monitor Low Energy Charged Particles during the Voyager '77 (originally Mariner-Jupiter-Saturn) mission. The two spacecraft probes in this series provide a unique opportunity for measurement of both the interplanetary solar winds and the local radiation fields of the two planets. The LECP is the latest in a series designed by S1P and includes an elementary Pulse Height Analyzer for improved particle identification and energy resolution. EME was responsible for the design and qualification of this Pulse Height Analyzer. Concepts, specifications and test results are detailed herein.

The LECP was conceived and designed by several individuals. The Pulse Height Analyzer portion uses some designs and concepts developed elsewhere in the experiment. The successful interface with the analog and digital portions of the experiment was due to the patience and perserverance of all concerned. Supporting help at the board and test level was provided by S1P and EEF fabrication personnel. Mechanical design and drafting was accomplished by S1P while the hybrid designs were developed within EME. JPL provided assistance in radiation hardening the design and maintaining highly reliable components for production. The attached references detail some of the contributions and the efforts of all concerned have been much appreciated.

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THE MJS LECP PULSE HEIGHT ANALYZER

A block diagram of the Low Energy Charged Particle (LECP) experiment is available as S1P drawing 1E0103 (check for latest revision), "BLOCK DIAGRAM Low Energy Charged Particle Experiment, MJS-77 Spacecraft". The Pulse Height Analyzer is centrally located and within the Pulse Circuit Assembly (PCA) on this drawing. This PHA monitors analog pulse inputs on the five lines D1 through D5 corresponding to particles incident on the LEPT detectors one through five. Additionally the PHA measures two DC levels shown as I alpha and I beta. The lines at the right of the PHA section are digital control and data lines interfacing with the experiment Command and Data Assembly.

During the journey to Jupiter, the experiment remains in the Low Energy Particle Telescope (LEPT) mode of operation. The PHA peak detectors are ON allowing measurement of four simultaneous detector outputs when requested by the DATA electronics. The short (typically 3 microsecond positive pulse) input signals are stretched for 1 millisecond to allow an analog to digital conversion of the amplitude. The A/D electronics produce 10 bits of binary code, the eight most significant of which are stored by the experiment data system. Either of the two redundant A/D converters may be used. Calibration is accomplished as desired to confirm internal operation.

As the Voyager encounters Jupiter, the Pulse Peak Detectors are turned OFF (data rate will be too high for effective operation) and the PHA monitors the leakage current of the alpha and beta detectors within the Low Energy Magnetospheric Particle Analyzer (LEMPA) portion of the experiment. All ten A/D bits are accepted by the data system providing resolution of 1/1024.

THE BASIC PHA

Refer to the Block Diagram Figure 2 and Data Timing Diagram Figure 3. The PHA is a fully redundant unit with the exception of the Peak Detector circuits. Independent control electronics, A/D converter logic, reference voltages and multiplexers allow operation with multiple failures in any one unit. This may be used to advantage if degradation of one PHA occurs during encounter with the Jovian magnetospheric radiation region.

The operating modes for either PHA are illustrated in Figure 3 by the Table of Output Data. Six sequences are possible for either PHA. A both OFF condition by command is also included, providing a total of 13 different operating modes. The operating mode is selected by three digital

lines from the Command and Data assembly to the PHA presently under power. The three signals, "Calibrate", "D1/D5 Select", and "LEPT/LEMPA" provide six output sequences since "D1/D5 Select" has no meaning when in LEMPA mode.

The main PHA power is switched to provide a very low standby drain (see the Table "Specifications"). Receipt of a "GO" pulse from the data section powers up the full electronics for the 1 millisecond measurement interval. The PHA turns itself back to Standby at the completion of the data conversion. The only external mechanism causing continuous PHA high power hangup is loss of "Clock". If this occurs, power may be removed by command.

The PHA is synchronized to the data system 50.4 KHz clock. The clock pulses control four timing lines in each PHA. These timing lines, "Busy", "A select", "B select", and "Output Time" allow serial data transfer during any arbitrary time interval. The A and B Select lines determine which of the four words is being shifted and the "Output Time" establishes the interval of data shifting. "Busy" signifies a measurement is being made. Data appears over a fifth line.

Figure 2 shows the interfaces. Five pulse inputs (to peak detectors) or two voltage inputs are to be measured. Five control lines provide a GO signal and mode control to the PHA under power. Two "PHA Power" inputs select either or no PHA (both ON is prohibited in external logic). Five output lines from the PHA in use supply timing information and data output to the experiment Command and Data section.

LEPT MODE

The five pulse inputs (D1 through D5) are shaped pulses from the LEPT section of the experiment. The pulses are generated by charge liberated in the corresponding Low Energy Particle Telescope silicon detectors as radiation penetrates the reversed biased junctions. This discrete charge produces a step voltage at the output of a Charge Sensitive Preamplifier which is further shaped to obtain a bipolar pulse (the pulse duration and shape being a compromise between noise level and count rate capability). The amplitude of this shaped pulse is a function of particle specie and energy. When compared with additional detector outputs from a collimated array (the conventional particle telescope) the amplitudes can be used to identify the radiation present. Therefore, an accurate measurement of the voltage peak can be used for analysis of the local particle population.

The bipolar pulse at the end of the amplifier cascade has a zero-crossing of about three microseconds. This signal is further processed by a logarithmic amplifier to obtain a dynamic range of up to 70db. The PHA peak detectors and A/D converters have a full scale reading of 2.0 volts with a resolution of 2 mV. The last two bits are not accepted by this particular experiment, thus the experiment resolution is about 8 mV. The PHA dynamic range of 1/256 (for 8 bits only) is expanded to 1/3000 by the previous log amplifier to obtain a constant percentage of reading accuracy. The combined processing allows detection of a 70 db dynamic range to 0.3 db resolution at count rates in excess of 100 pps.

Peak detection is illustrated by Figure 1. This simplified functional schematic and timing diagram shows required control and timing. The Peak Detector tracks the input signal and maintains the highest previous positive level until a negative going zero crossing occurs. The Zero Cross Discriminator triggers a 2 microsecond interval which opens the "Hold" switch.

The pulse that produced the peak and zero crossing is monitored elsewhere in the experiment logic. The two microsecond delay one-shot maintains the output of the peak detector long enough for the data system to decide whether a measurement should be accomplished on the pulse. If the particle appears to be of interest, the "external hold" line goes positive before completion of the two microsecond delay and maintains S1 open until the end of a measurement interval (about 1 millisecond). Note that S1 must be available since there is significant probability a large signal will occur during the 1 millisecond and the peak detecting diode would again conduct.

Once the data measurement is made, or at the end of the two microsecond delay in the absence of a measurement request, the six microsecond one-shot fires closing S2 and discharging the peak storage capacitor. The "hold" signal shown is generated within the PHA electronics, a "GO" pulse from the Command and Data section of the experiment sets the "hold" high and it remains there until a full conversion cycle has been completed.

Timing is arranged in the control circuits so that "hold" switch overlaps the reset signal and the amplifier does not drive the shorted output. The actual circuit allows any of the five D input lines to initiate the delay and reset cycle, each line having its own threshold discriminator. Thereby, if any line detects a pulse of interest, the levels measured at the other four peak detectors will be for the same instant in time (all "hold" switches open simultaneously).

Circuitry is described in detail later herein, the "hold" switch used for illustration has no physical identity, the amplifier is gated for continuous negative output voltage and isolation accomplished by the output diode. The "reset" switch is a JFET. Circuit values are critical in obtaining a fast enough slew rate to track the input waveform and retain sufficiently low leakage currents to maintain the stored peak voltage for at least one millisecond with less than a 2% droop.

Peak detector deployment is shown in Figure 2, "Block Diagram Pulse Height Analyzer". One is provided at each D input, no redundancy is used. Their outputs drive multiplexers to each of two redundant analog to digital converters. This is power and circuitry efficient, if one peak detector fails only one channel is lost. Any failure in the remaining electronics would kill the system if it were not redundant. Also the peak detectors are a major power consuming element of the PHA. Peak detectors may be commanded OFF as desired (i.e. LEMPA mode).

The timing described is faster than the basic operation of the A/D converter electronics which use the 50.4 kHz clock. Therefore, no attempt is made for precise timing between the event and data output. Timing signals are internally generated to be compatable with the data section.

The function described could not be implemented with commercial components available at the time of design. In house hybrid circuits were developed to achieve the power, accuracy, radiation hardening, and speed tradeoffs needed.

LEMPA MODE

The Low Energy Magnetospheric Particle Analyzer is used during encounter with the Jovian radiation belts. The counting rate is expected to be too high for useful peak detector operation which are switched OFF to minimize power and improve the radiation tolerance.

The "LEPT/LEMPA" signal in LEMPA mode switches the multiplexers to monitor the I alpha and I beta voltages. These are eight volt full scale and are directly proportional to the leakage current in the two corresponding detectors of the LEMPA. Details of the conversion from leakage current to voltage are provided in EME-75-227, "Current Monitors for S1P Mariner-Jupiter-Saturn LECP Program".

The same data timing cycle is used in LEMPA mode resulting in two cycles of the current data (see the timing diagram). This simplifies the electronics and is compatable with the Command and Data section which retains only a single reading. Command and Data has two changes in operation, it ignores one cycle of the output data and retains all ten bits of the conversion.

Three point calibration was provided in LEPT operation with measurements at 0.2%, 6% and 45% of full scale. Only two points can be accomplished for a LEMPA calibration and 0.2% and 98.3% are used to establish offset errors and scale factor. The actual calibration points were chosen to minimize circuit design and are not considered optimum from a transfer function view.

Summing up the basic PHA concept, the Pulse Height Analyzer is a subsystem featuring redundant control electronics with 10 bit analog to digital converters and 10 channel multiplex networks. In addition, five peak detectors with associated logic are provided for measurement of pulse amplitudes. The PHA is under control of the LECP experiment Command and Data electronics, performing a data conversion whereever a "GO" signal is received, in an preselected operational mode. It provides clock synchronized but time independent serial data readout with four timing lines in each interface. A complete conversion interval requires about 1 millisecond. Pulse peaks are measured as requested during the cruise portion of the mission (when in LEPT mode) and two detector average currents during the encounter (LEMPA) interval. Power may be commanded ON to one or no PHA control section and is ON for the peak detectors when either PHA is ON and in the LEPT mode.

CIRCUIT DETAIL

The PHA can be analyzed using the included block diagrams, timing diagrams and circuit schematics. The following comments are guides to the drawings and diagrams and include a number of unique areas encountered. A prototype tester is available with one set of the basic A/D converter and control boards, as of July 1977 no spare set of Peak Detector boards was available. The test set, test mounts and spare boards are in storage at the S1P electronics laboratory, Howard County, building 4, room 237.

The Pulse Height Analyzer consists of 10 printed curcuit boards in the Pulse Circuit Assembly of the Low Energy Charged Particle experiment. The boards include the following:

1520-1	Fast Comparator and Multiplexer for the #1 PHA.
1520-2	Same for the #2 PHA.
1530-1	Reference Voltage and Power Switching for #1 PHA including Peak Detector power switches
1530-2	Same for the #2 PHA but does not include Peak Detector switches. Line interconnects with the 1530-1 board to accomplish Peak Detector power during PHA-2, LEPT operation.
1540-1	A/D cycle logic with R/2R ladder drivers.
1540-2	Same as above for #2 PHA.
1550-1	Experiment interface and standby logic. Controls timing and performs logic level shift from 8V external to 12V internal.
1550-2	Same as above for #2 PHA.
1560	Peak Detectors and Discriminators.
1570	Buffer Amplifiers and peak detection logic control.

The 1520, 1530, 1540 and 1550 boards work together as a unit performing analog to digital conversion and multiplexing upon receipt of the experiment GO pulse. The 1560 and 1570 boards work together as five channels of peak detection with no interaction to the rest of the PHA except for power control and the HOLD function.

PHA TO EXPERIMENT INTERFACE AND CONTROL

The 1550 and 1530 boards provide power control, input line buffers, output line drivers and most of the logic necessary for the interface. The detailed block diagram of Figure 2 illustrates the power control structure wherein the major portion of the PHA circuitry stays OFF except during the analog to digital conversion cycle. Also, power to the peak detector and buffer boards (1560 and 1570) is on only when one of the A/D converters is under power and in the LEPT mode.

Power voltages are switched by either of two EME hybrids (0265 and 0274) as designed by D. Fort. These use J-FET switches to achieve efficient power control. Standby power is controlled by a type II (EME 0265) switch hybrid which is minimum power drain but slow switching. Cycled power for the A/D conversion cycle is controlled by a type III (EME-0274) hybrid and two transistors to obtain rapid turn ON (typically less than 3 microseconds) at the start of the cycle. Three types of power distribution are shown in Figure 2, the standby power as dotted voltages, conversion cycle power as "S" voltages, and peak detector circuit power as "P" voltages. In all cases the switch hybrids are turned ON by a positive voltage at the control pin.

The standby circuits of the main electronics are shown as the right hand portion of Figure 2 and are separated from the cycled power blocks by a vertical dashed line. This circuitry must accomplish the following:

PHA STANDBY CIRCUIT FUNCTIONS

1. Control power lines.
2. Provide master timing for conversion cycle.
3. Detect the request for a conversion by the "GO" signal.
4. Detect the operating mode from Cal, L/L and D1/D5 inputs.
5. Regenerate the 50.4 kHz clock for timing and provide two phases for internal operation.
6. Translate the +8 volt external signal levels to the +12 volt digital levels required for the A/D conversion.

Most of the control and interface circuitry is on the 1554 board. The schematic shows the interfaces are accomplished with hex buffers, inverters for the input control lines and non-inverters on the output digital lines. An exception is the clock detection Schmitt-trigger which is designed using three NAND gates. Schmitts were not available for this program. Logic level translation from the internal +12 to the required +8 V output is done directly by the CD4050 buffer. Input level shift from +8 to +12 is more difficult and required transistors Q1 through Q5. The transistor bias circuit for Q1 and Q5 uses a hot-carrier clamp diode (CR-1 and CR-2) to prevent saturation and maintain fast turn-off in the "Go" and "Clk" circuits. The transistor collectors have the same phase as the emitters and switch between about +0.2 V above the drive lower voltage and +12 volts. This logic voltage shift was done in the interest of using as high a reference voltage as practical (8.000 V) to minimize offset errors and noise during the analog to digital conversion.

Interface noise rejection is enhanced by the clock Schmitt-trigger and providing shaped transitions on the output lines. False clock pulses would be a major problem since they could cause internal logic state jumps and pronounced malfunction. Shaping the output transitions both reduces cross coupling in the cabling and minimizes ringing at the receiving end of the lines. The buffer inputs and outputs are all resistor isolated to prevent loading of the experiment Command and Data logic at times the PHA is turned OFF. Note the input lines do not have pull down input resistors and the board must not be operated without being connected to a tester or some other control to prevent excessive current drain in the U1 and U3 integrated circuits.

Conversion cycle control is accomplished by the binaries of the U6, U7 and U8 packages. The "Detailed Circuit Timing Diagram", Figure 5, shows most of the waveforms within the 1554 board.

CONVERSION CYCLE TIMING

1. A "Go" pulse (duration greater than 0.2 uSec positive going) arrives at some arbitrary time setting the "Run" binary.
2. "S" voltages are turned ON. The "Set" binary remains at 0 resetting the A/D converter binaries at the desired state as power comes up and the unit normalizes to the start condition.
3. The "delta" binary begins to cycle on the first positive going clock transition after the "Run" binary is set. Its output is clamped to 1 during standby and must transition to 0 and back to 1 to clock the "Set" binary. This generates a minimum of 1 clock time (abt. 20 uSec)

delay for the reset of binaries during power turn ON.

4. The "Set" transition from 0 to 1 removes the reset drive to the A/D converter binaries (via the Clamp gate of 1540) and the "A", "B", and "C" master timing divider. The A/D clock (i.e. "Gated Clock") begins to run. (Pin 11 of U-12 on the 1540 board).

5. The A/D converter cycle is controlled by a 12 step sequence generated by two CD-4017 10 step counters. The most significant bit @ 1 is maintained for the first two gated clock intervals. This allows between 4 and 5 clock periods (nominally 80 to 100 uSeconds) at power ON time to allow all circuits including the reference voltage to settle prior to deciding the most significant bit value. The scheme also provides a three clock period interval (about 60 uSec) for the multiplexers, amplifiers and comparator to settle when switching inputs for the second, third and fourth measurement.

6. The "Clamp" line of the 1554 board resets all "bit binaries" to 0 except the MSB and both 10 step counters to zero during the converter power ON, "Set binary" low interval described above.

7. The 1554 board "Reset binary" is originally clocked to 0 during the "Set" low interval. The "Gated Clock" steps the U9 10 counter through its 10 step sequence. The positive transition of its "0" step output toggles the "Enable" binary which generates an immediate count to U11. The next positive clock transition after U11 reaches the "2" condition causes the "Reset" binary to go to 1 generating a "Clamp" and resetting both 10 counters back to zero.

8. The positive transition of "Clamp" drives the "A", "B" and "C" master timing chain. The "A" and "B" levels select the multiplexer position (in conjunction with additional experiment inputs). "C" is used to shut down the A/D converter after the fourth channel is finished.

9. Note that several short delays are required in the circuitry to prevent signal "race" problems. These are shown in Figure 2 as circled delta symbols. For example, it is necessary to maintain operation for one clock interval after completion of the fourth data comparison. The fourth positive transition of the "clamp" signal causes the "C" binary to to Hi, the output is delayed a fraction of a microsecond to insure the D input to the "Run" binary changes after its phase 1 clock transition thus requiring one more clock interval prior to conversion power turn off. All logic is stepped in phase 1 clock time, the phase 2 clock is provided to allow gating, phase 1 is restored at the point of clocking.

10. The "Run" binary remains at 0 until a new "Go" pulse occurs. "S" power lines are OFF. Multiplex power is OFF and the Peak Detector "Hold" is removed. The delta binary is set to 1 and the "Set" binary reset to 0. "A", "B", and "C" are clamped at reset.

11. The "A", "B", "O.T.", "Busy", and "Data" logic levels are supplied to the experiment Command and Data section. "O.T." is the "Output Time" signal indicating good data is present. Note it is offset one clock time from the "A" and "B" multiplex control levels because the data is strobed at the end of each comparator clock interval. This requires an adjustment in the experiment data section to correlate the bits. The "Busy" level indicates a conversion is in progress.

12. The entire cycle for four channels of data takes about 910 microseconds at the nominal 50.4 kHz clock rate. There is no way to terminate a cycle once it is initiated. Loss of clock will cause the conversion cycle power to remain ON once a "Go" signal is received. This can be removed by commanding that PHA (1 or 2) redundant section OFF.

During the cruise phase of the satellite mission, the peak detectors will be powered as part of the LEPT (Low Energy Particle Telescope) mode. These have their own synchronous timing as illustrated in Figure 1. The peak detectors hold the most positive voltage input since the last zero crossing of the analog channel, hesitate for 2 microseconds at the next zero crossing and reset to zero. The experiment data section has 2 microseconds to request a PHA reading by generating a "Go" pulse after which time the PHA logic maintains the peak values for the duration of the total A/D conversion, nominally 910 microseconds. The only control circuits required for the peak detectors are the "Go" detector, "Set" binary and its "Hold" output. Reset is generated for all peak detectors by any of the five inputs making a negative going zero crossing after exceeding the threshold of its discriminator. Reset also occurs at the end of a conversion cycle when the PHA hold level returns to 0.

A/D CONVERTION

Most of the converter circuitry is on the 1522 (Fast Comparator and Multiplex) and 1540 (A/D Converter Logic) boards with an additional two binaries on the 1530 board. These circuits are the Cycled Power section of the "PHA-1 Detail" in Figure 2. Multiplexing of signals will be discussed separately. The input to the A/D converter is defined as the output of the hybrid inverter amplifier (EME 0269) U4 of 1530 which is -8.0 V full scale in all cases.

A/D conversion is accomplished in successive approximation using a Micro Networks Corporation MN-121 12 bit R-2R ladder network. R is 50 K ohms which is compatable with the CMOS drive circuitry and minimizes current drain. Only 10 bits are used, the device is overspecified to improve the long term stability. The ladder is a thin film nickel chromium array of 12 bit accuracy over the standard military thermal environment. The absolute accuracy of the resistors is only 10%, however the comparison resistor is included in the array providing the required .05% matching accuracy with a relative temperature coefficient (tracking between resistors) of about 1 ppm/ °C.

An 8.000 volt reference circuit is designed around an EME-0270 hybrid and a 1N4568A 6.4 V precision zener. The amplifier is designed to turn ON and settle to within 1mV of final value in less than 10 microseconds. This saves considerable standby power. An absolute accuracy of 2 millivolts or better was desired to minimize package calibration and allow board interchangability. Another hybrid, the EME-0266, is used for feedback trim and establishing the reference level. This is somewhat similar to the Micro Networks package in that the absolute resistance is not very accurate but the temperature tracking is excellent. Resistance is specified as 20% or better with the ratio of taps maintained to better than .05%. Careful layout produced an excellent thin-film array, one of the few produced to have a 100% yield over the full thermal environment. Thus, the reference level is adjusted to within 2 mV after the 1530 board is completed by jumpering the necessary taps of the 0266. The 1N4568A reference zener is specified as

less than 10 mV shift over the full military range with a T.C. of .001%/°C. This drift can be halved by going to a 1N4569A at a significant increase in cost. For a ± 50°C environment, the drift contribution is equal to that of the feedback divider.

Figure 4 shows a block diagram of the analog portion in the A/D converter. Total error will be discussed under "Multiplexers". Amplifier analysis is available in the memo EME-75-201, 19 August, 1975, "Hybrid Level qualification of the EME-0270 Positive Output Op Amp." The 10 bit system has the LSB @ 8.000/1024 or about 8 mV. The flight boards were individually tested thermally producing the following results of reference voltage stability.

8V REFERENCE VOLTAGE FOR THE LECP PHA

			-50°C	ROOM	+50°C
Prototype	1 Sept. 76	PHA-1	7.992 V	8.000 V	7.999 V
		PHA-2	7.988	7.998	7.998
Flight 1	16 Nov. 76	PHA-1	7.990	7.999	8.005
		PHA-2	7.996	7.997	8.000
Flight 2	20 Dec. 76	PHA-1	7.996	7.996	8.000
		PHA-2	7.989	7.998	8.005

The above measurement included all sources of temperature dependence, the zener, amplifier offset, and precision divider. Note the lower temperature is considerably colder than the expected operating limit of the experiment.

Reference shift with input voltage is also of interest. The +12 V "S" line is probably the most significant. For the same units the following measurements were made.

8V REFERENCE OUTPUT FOR ± 10% INPUT POWER (ALL LINES)

		-50°C		ROOM		+50°C	
		-10%	+10%	-10%	+10%	-10%	+10%
Proto	(1)	7.991	7.995	7.998	8.002	7.997	8.000
	(2)	7.987	7.989	7.997	8.000	7.996	7.999
Flt. 1	(1)	7.987	7.992	7.997	8.004	8.004	8.009
	(2)	7.995	7.997	7.997	8.001	8.001	8.003
Flt. 2	(1)	7.995	7.997	7.996	7.998	7.998	8.001
	(2)	7.988	7.991	7.997	NA	8.002	8.006

The above shows the reference accuracy is sufficient for a 10 bit absolute measurement at any one temperature with a one bit uncertainty over the thermal range. In conjunction with other error sources this suggests the use of individual calibration for each PHA over the environment. However, in the LECP the PHA thermal shifts are small with respect to the signal processing chain, especially the logarithmic amplifiers, and overall calibration is a better method of maintaining total available accuracy.

The comparator circuit is designed around discrete components and included in the schematic of the 1520 board. The configuration is similar to that of the hybrid amplifiers with an input JFET matched pair driving a PNP current mirror to produce very high input stage gain. For positive input voltages the left hand JFET is more conductive thus driving pin 7 of Q1 into saturation, clamping the following PNP OFF with a resulting high output at the "HI/LO" output. As the voltage drops below zero the unbalance in current drives Q3 causing a voltage increase at pin 14 of the CA3045 NPN transistor array. Pin 5 begins to drop in voltage. Positive feedback to the R32-R37 divider drives the pin 11 current reference and about 2 millivolts of hysteresis is produced. C5 is used to maintain a controlled output time constant of about 0.4 microsecond. The comparator could be fabricated as a hybrid, it is not from a cost savings view as only one per A/D section is required.

The case of U4 is grounded to minimize noise pickup. The input Z at pin 7 is 50 kohms and susceptable to strays coupled through the case itself. Stability of measurements improved noticably after the case was grounded with last bit uncertainity approximating statistical randomness when the voltage is near the transition point for the next bit.

U5, a five transistor array from RCA, provides not only the high-speed NPN units for the comparator, but clamping at the input (pin 7 of Q4). The diode is the substrate to collector diode of the adjacent transistor thus obtaining both positive and negative clamp of the input signal with no additional components. The diode wired NPN across the collectors of Q1 prevents the voltage on Q4-2 from dropping more than about 1.2 V below the positive bus thereby maintaining speed in the comparator by holding the 2N5564 in the pentode region and preventing Q3 from saturating. R39 isolates the comparator from its load and protects the output stage.

The comparator is tailored identically to the hybrid operational amplifiers, additional DC current is added to the PNP mirror (with the appropriate phase) to trim the balance point to less than about 1mV. This is done dynamically in the flight boards. The U4 hybrid amplifier is trimmed statistically for less than 1 mV output error with pin 1 and 12 of U1 shorted to ground and the tester setup for LEMPA operation (i.e. the U1 multiplexer is connected with U2 and U3 clamped at the #1 or zero volt input terminal as will be discussed later). The tester is then setup to CAL LEMPA and allowed to run. The comparator is trimmed to the middle of the resistance range that holds a channel 1 readout of 0002.

Note the trim voltage is marked as +12F. This is capacitively coupled to the +12 V input by 1ufd (C14) of the 1530 board. This reduces the power line noise coupling of the trim resistor, otherwise all noise components will drive the PNP's (Q1) directly against the trimmer. The same technique is used with U4. The coupling rolls off below about 17 Hz. A better arrangement for future designs is to put the bias AC coupling directly at the emitters of Q1 and R42.

The U4 hybrid amplifier is used to scale the input level and invert it. The scaling resistors are in series with the three multiplexers and set the gain in reference to the 120 kohm 1/4% feedback resistors of U4. The negative output is needed for comparison with the positive drive from the U6 R/2R ladder network. The ladder is driven from COS-MOS hex buffers powered from the 8.000V reference supply. Thus when the total current contribution from the ladder binary segments equals the current from the inverting amplifier U4 (as

determined by the U6 internal summing resistor between pins 15 and 16) a null balance occurs. A successive approximation technique is used wherein the most significant bit is originally set to unity (with the remainder to zero volts) and each successive bit energized. The circuitry keeps each bit high if the comparator detects a negative input (i.e. not enough voltage) and resets it to zero if the comparator detects a positive level (too much voltage).

A/D CONVERSION TIMING CYCLE

0. At the initiation of a GO signal, the A/D power is turned ON and the first measurement is maintained in the MSB HI state for 4 to 5 clock periods (80 to 100 microseconds) while power transients normalize. Control circuits are shown on the ID 1540 schematic. The Data Clock is running and U9 (1 of 10 counter) is stepping.

1. U9 of ID 1540 reaches the "3" output (pin 7) which sets U2 pin 13 HI and clocks U2 pin 3. The second bit is high and the MSB is clocked HI or LO depending on the state of the comparator. A delay of about 440nSec is introduced in the clock to the MSB to insure sufficient time for the previous set to clear (this is not really necessary for the MSB since that input does not remain high during the first three steps of the 1 of 10).

2. The sequence continues until U9 has completed all 10 steps and is back with the 0 output (pin 3) just transitioned to HI. This clocks the ENABLE binary U10-1 to the Q2 LO so that at the next clock ing the U11 1of 10 counter and causing it to step to the 1 output.

3. The sequence continues until U11 steps to the 2 output (pin 4). This sets D of the Reset binary HI so that at the next clock positive transition U10-13 goes HI causing a reset pulse. Both steppers are reset to 0 and the Enable binary again selects U9.

4. Three clock intervals are required until U9 again reaches the 3 output and the next most significant bit is set. This extra duration allows the multiplexer and inverting amplifier time to settle as the new analog channel is selected. Note the Reset pulse caused a Clamp pulse which also clocks the master A, B and C timing flip-flops advancing them to the second state.

5. The sequence continues to cycle until four multiplex channels have been converted and the fourth clamp pulse causes conversion power shut off as previously described under "Conversion Cycle Timing".

Note that the number of buffers driving the R/2R ladder are variable. The first two most significant bits have three each, the third uses four in parallel. This compensates for the variation in ON resistance from one hex buffer to the next, the error in the first two bits should track while that in the third may jump. The 50kohm resistors in the ladder require less than a 500 ohm drive resistance for 1% accuracy and less than 50 ohms for .1% absolute accuracy. The buffers are typically 200 ohms resistance when HI at 25°C but may be as poor as 600 ohms. Therefore, there are two important considerations, absolute accuracy and monotonicity. Absolute accuracy is not as important as monotonic output since the actual response must be calibrated anyway (the analog channels having the major uncertainity). Although no problem was detected in any of the six flight units, it appears there could

be a nonlinearity if the worse combination of buffers between the three were applied and for critical applications it will be useful to check their characteristics prior to circuit fabrication, using the lowest value of r as U1, next as U4 and highest for U7. If allowable, a future design might use quad switches such as the CD-4066, biased at 12 V and switching the 8 V reference to obtain consistently lower impedances. Three of those packages would have 12 switches allowing two parallel for the first two bits for a typical 50 ohm ON resistance at the two most critical points. An even better switch is the Harris Semiconductor HI-5051 which is 50 ohms maximum over the full military temperature range and 25 ohms typical at room temperature. These are logically compatable but only contain two DPDT switches per package so that 5 are required for the full complement. They could replace U1 and U4 only with no increase in package count.

Figure 5, "Detailed Circuit Timing" shows the A/D converter sequence. Note again that the multiplexing signals are generated by the "A" and "B" master counter and the output data runs one clock time behind the bit under conversion. The "Output Time" level is synchronized with the data and instructs the experiment Data logic to read the output, however the "A" and "B" levels change at the least significant bit which complicates the data storage. This could be improved on future units by adding two binaries to provide a one clock time delay in the "A", "B" readout.

MULTIPLEXING

Multiplexing is shown on the schematic for the 1520 board. One dual four channel multiplexer (U1) is used with its switches paralleled as the LEMPA mode current monitor multiplexer. The third and fourth switched points (pins 5/15 and 1/12) provide calibration inputs. Two 1 of 8 multiplexers are used for LEPT mode multiplexing (U2 and U3) with the second four inputs used to select the normal data for either D1 or D5 mode and the first four input points selecting the calibrate sequence. This is efficient in circuitry since the outputs of all three multiplexers are always summed. Thus two of the $\overline{U1}$, $\overline{U2}$, $\overline{U2}$ lines are clamped to ground under any operating mode holding their respective multiplexers at the "0" input points while the third is high allowing its multiplexer to be scanned as the "A" and "B" lines count. The "C" input selects the normal or calibrate condition. U2 and U3 are grounded on their "0" input point producing no offset while U1 is providing LEMPA data. U1 has about 16 millivolts at its "0" input point for use as a 0.2% reference level during LEMPA calibration. LEPT mode uses only 8 of the 10 available bits with a resolution of 32 millivolts so that U1 introduces a constant 1/2 LSB offset in the data which is considered trivial. This error may readily be corrected if required, for example the R10 calibration resistor might be replaced by two in series of 50kohms each with a diode at the center tied to the $\overline{U1}$ logic control line thus reducing the offset during LEPT mode to less than 2mV. Or the R10 resistor could be driven from the $\overline{U1}$ line directly since an accuracy of about 25% is sufficient at this low calibration level.

Multiplexer selection is determined by the state of the LEPT/LEMPA (L/L) level, and the D1/D5 select level. The L/L input sets the $\overline{U1}$ control LO when L/L is HI clamping the U1 multiplexer (board 1524) to the "0" condition. A HI D1/D5 input clamps the $\overline{U3}$ control LO selecting the D1 input signal. The $\overline{U2}$ control is LO if D1/D5 is LO selecting the D5 input signal. The calibrate input drives all three multiplexers selecting the 0 through 3 inputs of U3 and U2 and the 0 and 1 input of U1 if HI (calibration mode) and the 4 through 7 inputs of U2 and U3 and 2 and 3 of U1 when LO for normal mode. The four steps during a readout are generated by the "A" and "B" binaries which control the U2 and U3 multiplexers at their A and B inputs. Only the "A" level is used

for the U1 multiplexer generating two repetitive cycles of the data.

Multiplexer power is switched from a hex inverter (pin 12 of U4, ID-1554) to obtain a low impedance ground during standby conditions for enhanced radiation resistance. In addition, the V_{SS} line is switched to -1.2 V when ON (at the recommendation of JPL to further harden the circuit). All inputs are resistor isolated since they will be continuously driven from the Peak Detectors (if in LEPT mode) and Current Monitors. The small capacitors in the signal lines are used to minimize noise coupling while maintaining sufficient settling speed.

Figure 4 shows the analog errors in the A/D conversion and Multiplexing. The multiplexers are just low enough in ON resistance to accomplish the desired accuracy of 1% in LEPT and 0.1% in LEMPA mode which is a major contributor to the difference in accuracy. The TRW 1/4% resistors are small components with excellent stability but will require slight trimming with additional series resistance if true 0.1% absolute accuracy is ever desired. Refer to the Calibration Table for the measured environmental characteristics of the six units fabricated.

The Calibration Table (page 23) is interesting. A comparison of all the data and the Figure 4 Error Block Diagram suggests the test system was introducing an offset error of about -10mV. This probably occurred in the ground return lead between the boards under test and the test control boxes. The test offset error is needed to explain the inconsistency between the calibration readouts, measured most significant bit values, and measured total reading offset. The Error Diagram suggests a maximum gain error for the MSB of about 0.7% with the LEMPA commutator. The MSB is expected to have a value of between 3.972 and 4.028 volts so that the measured values are reasonable. The comparator is tailored to establish a LEMPA 0.2% calibration of 0002 counts which corresponds to an input of 15.7 mV ±4. This establishes a room temperature offset voltage of less than 4mV and probably less than 2mV overall since the tailoring is adjusted for the center of the correct readout. Thus the measured system offset is inconsistent. Future tests should be accomplished with both voltmeter leads routed through independent wiring to the circuit board inputs rather than at the Tester output.

The multiplexing circuit introduces uncertainity as illustrated in Figure 4, "PHA Basic Error Block Diagram". The ON resistance of U2 and U3 is 200 ohms or less which is about 0.7% of the total input drive resistance to the U4 inverting amplifier during LEPT Mode. The input isolation resistors are 10k ohm 1% contributing an additional 100 ohm uncertainty. These errors are not significant with respect to the uncertainity of the prior analog signal processing and should shift only a fraction of the absolute error with temperature. Checks of the three units fabricated to date show typical tracking errors across the multiplex of 0.2% with one channel showing close to a 1% error over the environment.

LEMPA operation is more critical since all 10 bits are used and the accuracy is enhanced by providing a greater input voltage (8 V instead of 2 V full scale) and lower multiplexer ON resistance. The major absolute error is contributed by the 1/4% MAR-3 resistors, however this remains constant over the channels. Relative error between channels amounts to 100 ohm from the 10k 1% resistors and the multiplexer deviation. Measurements show consistently better than 0.1% channel to channel tracking over the environment in the LEMPA mode.

Note that the Error Diagram does not include the ladder driver error, which can be important, as previously discussed.

PEAK DETECTOR CIRCUITRY (LEPT MONITORS)

The Peak Detector Circuitry and the associated logic is shown as the Schematic for the PHA 1570 board. The EME hybrid design is discussed in EME-75-186, "Hybrid Level Qualification of the EME-0267 PEAK DETECTOR". The interface with the remaining PHA circuitry is illustrated in Figure 2, "Block Diagram, Pulse Height Analyzer".

Each of the five logarithmic analog inputs from the experiment LEPT section (D1 through D5) drives a peak detector hybrid and a discriminator hybrid as shown in the block diagram. The peak detector has a 100nSec time constant in the positive direction and a dynamic range of at least 0 to 2.0 volts. The schematic is given as EME-0267, "Schematic Diagram". It includes a 5000pfd NPO amplitude storage capacitor (C3) and a 2N4858 reset FET (Q5). The "Hold" function is accomplished by biasing the #3 pin to one diode drop above the +6 V power bus, thus keeping Q4 OFF and removing drive from the output transistor and diode. The output will be driven up to the maximum value of the input level during normal operation with positive inputs, held at that value for one millisecond during a data conversion when requested and reset for about six microseconds after data conversion or two microseconds after the next zero crossing if no data is requested. The delay and reset timing is generated on the 1570 board which also mounts the buffer amplifiers.

External 33Megohm bias resistors were added after test showed some of the hybrids would drift positive when cold. This is inherent from the N channel input differential FET as the gate leakage charges the output capacitor. A diode (CR1) is provided in the hybrid to generate a net negative current at the feedback node, however the temperature coefficient of the diode is greater than that of the JFET's in some cases resulting in the positive drift. The 22 Mohm resistors held at -.55 V bias cured the drift. They create a time constant of about 10^{-1} second or about a 1% discharge in the required 1mSec maximum conversion interval. The JFET's were selected for a low gate leakage which is typically 20 picoamperes at 25°C. Note that the output capacitor is connected to two JFET's, one in the peak detector and another in the following Buffer Amplifier (EME-0268). The 22Mohm resistor is the largest value obtainable at the time of fabrication, a larger value of up to about 200Megohm would introduce less error, a constant current drain of about 2nA for zero output. This would be especially effective if a temperature dependent bias voltage were used to compensate as the JFET leakage increased hot. Maximum gate current at 25°C is specified as 100 picoamperes.

The Peak Detector is tailored for minimum offset voltage error. The least significant bit used in LECP operation is the 8th with a corresponding value of about 10 mV at the Peak Detector. Full scale is defined as 2.0 volts which allows for operation from -50 to +50°C and ± 6.0 V + 10% on the power supplies. If larger inputs are required, the positive power supply voltage should be raised accordingly in order to maintain the FET's in the pentode region and keep the offset balance error to less than 20 mV deviation. The manufacturer specifies less than 1 mV balance change over the temperature environment which corresponds closely to the 2 mV change noted for both Peak Detector and Buffer in the flight units. Note the thermal drift is minimized if the original trim is accurate and the room temperature offset at about 1 mV or less.

The following table of characteristics summarize the peak detector hybrid:

EME 0267 CHARACTERISTICS

Input current:	-100 picoamperes max @ 25°C
Offset Voltage:	Trimmable to less than 1 mV, 1 mV max shift with temp. 20 mV worse case shift at 2.0 V input, +50°C and +5.5 volts power.
Output:	Zero to 2.00 V from 1K ohm in series with 5000 picofarad.
Reset:	To within 2 mV of ground within 3uSeconds @ 25°C, linear with absolute temperature.
Reset drive:	-6 V for OFF, +0.6 V for Reset.
Hold:	Amplifier unbalanced, will ignore up to +5V input.
Hold drive:	Ground for normal operation, +0.6 V above +6 V bus for Hold.
Output drift:	Supply external pull down current of 2nA or greater to assure no positive drift at cold temperatures.
Hold drift:	Will maintain 1% or 6 mV over 1 millisecond at output during hold if external load (Buffer Amplifier) is less than 2nAmp.
Tracking Speed:	Output time constant of less than 150 nanosecond.
Power required:	+6.0 V @ 1.6 mA ±0.2 -6.0 V @ 1.6 mA ±0.2
Special requirement:	Bracket "Reset" time with "Hold" time to prevent high power currents.

The EME-0262 discriminator hybrids are used to determine the negative going zero crossing after a minimum height pulse in order to generate a reset pulse after a 2 microsecond delay. These use RCA transconductance amplifiers which require up to 7uA input current from the D lines. A limiting 510 ohm resistor is provided in series with the inputs for protection of the drive circuitry, especially during the time the PHA is in LEMPA mode and all Peak Detection circuitry is unpowered. The discriminator input current can generate up to 3.5 mV additional offset error at the Peak Detectors and will contribute to the temperature shift. The amount is not significant in this application but can be eliminated in future designs if warranted by using separate input lines for the Peak Detectors and Discriminators with individual limiting resistors. Note the present 1560 boards are tailored for offset after fabrication and a discriminator with the maximum specified input current may generate a problem with offset shift vs. temperature.

The discriminators are adjusted individually for desired threshold point according to the relationship:

$$V_T \approx 1.3 \times 10^{-4} \; R_T \Big|_{V_T < 0.5V}$$

Each unit is slightly different so that individual tailoring is required. The values for the threshold levels are chosen to minimize detection of background noise (which would otherwise reset legitimate signals in other channels) while detecting the same lowest amplitude as the LEPT discriminators. The levels remain fixed. If future experiments use channels with variable minimum detection levels (as has been incorporated in a number of past devices) the Peak Detector Discriminator levels should track the main channel levels to prevent data error. Otherwise an error can occur if the PHA retains a larger pulse than the main channel minimum detection level but lower than the PHA discriminator setting.

The 1570 board provides five buffer amplifiers (EME 0268) to follow the Peak Detectors with minimum current drain (same input specs as Peak Detectors). The peak timing logic is also on the 1570 circuit. Figure 1, "Simplified Peak Detector Block Diagram", illustrates the logic operation. The five discriminators on the 1560 board drive the U7 NOR gates so that any one making a positive to negative transition (which occurs at zero cross following a detection) produces a positive transition at pin 14 of the U8 dual one shot (EME-0263B). This clocks the internal D flip-flop and initiates a 2 microsecond positive output at pin 13. The U7 pin 10 NOR gate produces a positive transition at pin 11 of U8 whenever all three inputs go to ground thus generating the 6 microsecond reset signal. Thereby if a "Hold" positive level is received from the PHA "RUN" flip-flop during the 2 microsecond delay interval, the Reset does not occur until the "Hold" level returns to ground about 1 millisecond later. The pin 10 output of U7 also drives the U6 pin 10 NAND to generate the Peak Detector Hold signal at board pin 29. This signal is delayed using the RC output network and the U8 pin 10 discriminator of the 1560 board in order to bracket the following Reset pulse. The discriminator threshold is set at 6.33 V with hysteresis dropping the negative threshold to 5.0 volts. The RC delay maintains the Hold function during the time the Reset pulse initiates (note the output of U6 pin 10 may exhibit a short negative spike as the U7 pin 10 output goes high and the U8 pin 9 output has not yet transitioned low) and stretches the Hold past the completion of the Reset interval by about 0.5 microsecond. The pulse timing is illustrated both by Figure 1 and in more detail at the board level on the 1570 schematic.

The buffer amplifiers (EME 0268) have two parallel outputs, each having an internal 1kohm protect resistor to prevent loading by the OFF section of the redundant A/D converters. They are also trimmed for minimum offset voltage after board fabrication and this is usually performed in conjunction with the 1560 board for best overall output offset. Their specifications are essentially a low input current unity gain follower and are discussed in more detail as part of EME-75-193, "Electrical Test for EME-0268, Unity Gain Buffer".

In summary, the Peak Detector circuitry uses five Peak Detectors and five Buffer Amplifiers to provide two outputs for each of the five D logarithmic channels, one for each of the two redundant A/D converter multiplexers. In addition, the two circuit boards (1560 and 1570) include logic and detection components to automatically reset the previous peak values two microseconds after a detected channel makes a negative going zero crossing unless a "Hold" level is received from either A/D converter at which time the detectors remain in the hold condition for the 1 millisecond data conversion interval. The following table of characteristics is useful.

PHA PEAK DETECTOR CIRCUIT SPECIFICATIONS

Power Requirements:	+12.0 V @ 4mA 8.0 @ 7mA 6.0 @13mA - 6.0 @23mA
Peak Dynamic Range: and Accuracy	2.00 V Full Scale, 20mV max shift from -50 to +50°C with 10% power deviation. Error increases rapidly above full scale as JFET's depart from pentode region. Use higher voltage on +6 V line for greater range. Will detect positive peaks only.
Storage:	About 1% max droop in 1 millisecond. Has 5000 pico-farad output.
Reset:	Within 2mV in 3 microseconds.
Reset Duration:	May be tailored, 6 microseconds in present system.
Delay Duration:	May be tailored, 2 microseconds in present system.
Channel Discriminators:	Set as desired, see Table on 1560 schematic.
Tailor points:	Peak detector offset volts Buffer amplifier offset volts Delay time Reset duration
Off Characteristics:	All inputs and outputs resistor protected.

The following improvements might be useful in future designs of the Peak Detector circuitry:

1. Speedup of the EME 0267 hybrid by eliminating the internal C2 stabilizing capacitor and series R4 output resistor. This should be thoroughly evaluated to determine if significant overshoot can occur, but may be a very cost effective improvement since no new substrates would be required.
2. Use independent input drive of the Peak Detector and Discriminator hybrids to eliminate offset errors from the Discriminator input current and allow larger protective resistors.
3. Use a higher positive voltage on the Peak Detectors to increase the allowable dynamic range.
4. Design a better pull-down bias network for the Peak Detectors to increase the storage time and eliminate the internal CR-1 pull down bias diode.

The above changes may allow overall operational accuracy of a couple of millivolts over the full environment. A very high speed detector (less than 1 microsecond total pulse half-width as previously discussed with SIP group) will probably require two peak detectors in series, one to quickly set the peak voltage and a second to provide the required long storage. The cascade allows a small storage capacitor in the first detector to quickly assume the desired peak and a larger capacitor in the second detector to charge slowly (over perhaps one microsecond) but maintain a small error with a realistic load (following buffer amplifier).

One additional system change is possible, at present the reset after a data conversion occurs at the end of the A/D conversion cycle, resulting in an additional 10uSec dead time (out of the 1000 microseconds conversion interval). Reset could occur one clock interval (20 uSec) earlier so that the system is immediately ready for another pulse, however, the improvement in dead time is rather small and requires an additional gate in the A/D control logic to cause Reset at the time the "C" binary switches high.

A primary reason for the hybrid amplifiers in the Peak Detector circuitry is the radiation sensitivity of all monolithic linear amplifiers and comparators evaluated and the severe environment of Jupiter encounter. Other applications with more benign conditions may favor the adaption of monolithics at a significant cost reduction.

TAILORING THE PULSE HEIGHT ANALYZER

The following points must be individually tailored after board fabrication:

1. Peak Detector offset voltages
2. Buffer Amplifier offset voltages
3. Discriminator threshold levels in peak detector circuits
4. One-Shots of peak detector circuits
5. Negative output amplifier of A/D converters
6. Reference voltage for A/D converters
7. Fast comparator offset voltage in A/D converters

Tailoring is accomplished on the board tester using extenders to allow board plug in to the connector mounts. Typically a set of A/D converter boards is tailored and tested as a unit although the boards should be interchangable upon completion. The Peak Detector boards have a separate test chassis and are tailored as a set of two.

A/D CONVERTER TAILOR

The A/D converter contains four boards as follows. A complete PHA has two redundant sets of A/D boards which are identical in pairs except for the 1530 board. The 1530-1 includes the U4 EME-0265 FET power switch and associated components for controlling the Peak Detector circuitry power while the 1530-2 board does not have those components mounted.

1520 Board	Fast comparator and MPX. Tailor U4 and Fast Comparator offsets.
1530 Board	Reference voltage and Power switching. Tailor Reference Voltage.
1540 Board	A/D cycle logic and ladder drivers. No tailor points.
1550 Board	Experiment interface and standby logic. No tailor points.

PEAK DETECTOR TAILOR

1560 Board	Peak Detectors and Discriminators. Tailor offsets and thresholds.
1570 Board	Buffer Amplifiers and peak logic. Tailor offsets and one-shots.

In the following descriptions, the boards are connected to the test chassis and controlled by the PHA test set. Each has been inspected and every resistor verified with a low voltage digital ohmmeter prior to tailoring. Confirm power currents are normal and voltages correct. Refer to the Layout drawings to identify components and pins on the boards.

1520 BOARD TAILORING:

Set the Test Set controls to LEMPA MODE, CAL, VERT MAN STEP. This kills the clock input and holds the PHA in the conversion cycle at channel 1, the 0.2% calibration input. Power currents should read the conversion values. Short pin 1/12 of U1 to ground to provide a zero input voltage for U4. Trim U4 for minimum offset voltage (less than 1mV at pin 15, be sure to reference the DVM

ground at the board) by adjusting R43 and connecting it to either pin 3 or 5 for positive or negative corrections respectively. Install the required resistor and jumper then retest to confirm the offset. Remove the short at pin 1 of U1 on completion of this test.

After trimming U4 the Fast Comparator offset is corrected. This circuit uses current trim into the Q1 PNP current mirror (so do all the hybrids). The current corrects for two primary errors, the offset voltage of the 2N5564 JFET pair (which is specified as less than 5mV) and the base emitter offset voltage of Q1. The sensitivity is about 30uAmperes trim current for 8mV (one bit) shift at the comparator input and varies with the transcoductance of the JFET's. R35 will cause a positive deviation (more input voltage at the detection point) while R36 generates a negative deviation. 100kohms at either point should cause about a 26mV shift. Note the reference point for the tailor resistors is AC coupled to the +12 V bus to minimize noise as previously discussed.

Fast Comparator trim is defined as setting the LEMPA channel 1 0.2% calibration readout at the center of the second bit (reads 0002). Set the Test Set for normal operation in LEMPA MODE, CALIBRATE. Observe the channel 1 readout during the tailor operation. Determine the current required to shift the readout to a reading of 0001 and also 0003. Define a current through R35 as negative (readout counts will drop) and through R36 as positive. Use 11.4 volts as the voltage across a total resistance of R_T + 10kohms. The desired trim current is then the median of the two values calculated. Install the calculated trim resistor and confirm its value by checking the additional current now required to shift the calibration to 0001 and 0003. An identical current of about 14uA into each tailor node should shift the bit, therefore a resistor of about 500kohms (22uA injected) should shift the count back and forth when connected across R35 and R36 respectively. The resistor value will vary with the transconductance of the JFET's. An initial error of less than 1mV is desired corresponding to about 4 uAmp uncertainty.

1530 BOARD TAILORING:

There are three adjustments in setting the Reference Voltage. Trim is provided for the CR-1 reference zener bias current, U1 offset voltage, and precision divider U2 voltage feedback. The completed board will have a reference output of 8.000 V ± 5mV.

The PHA Test Set is set to the LEPT mode and VERT MAN STEP to keep the A/D converter circuit under continuous power.

R4 will have been originally installed as 3.0k ohms. Measure the CR1 reference voltage directly at the board with a DVM. Calculate the R4 range which will maintain a bias current of 500uA ± 50uA and have R4 changed if the 3.0k ohm value is outside the range.

Connect the DVM directly across the U1 pins 7 and 9. Adjust the R1 tailor resistor for an error of less than 1mV.

Monitor the Reference Voltage using the board pins and short sections of the U2 Precision Divider until a value of 8.000 V ± 4mV is obtained. Have the jumpers installed and confirm the trim. Note, it may be necessary to install the more significant jumpers prior to making the fine adjustment for best results. Read the reference voltage at the test control box and note the error introduced by the test wiring.

PEAK DETECTORS, 1560 BOARD TAILORING:

This board may be monitored by using miniature test hooks cut for the smallest practical hook. The hooks will easily pick-up individual hybrid leads for monitor. Short each input at the board when adjusting the voltage offset errors and keep both DVM leads at the board pins. Set the control box to "Hold", allow the output of the peak detector to drift negative, then release the "Hold", and observe the zero reference output. Less than 1mV error is required for each of the five peak detectors. Use the schematic and layout drawings to identify the required monitor points and tailor resistors. Allow the board at least one minute to warm up prior to attempting adjustment and confirm each offset and record after the desired resistor is installed. The original value may be determined using either a decade box or individual MEA resistors, the short leads of the discrete resistors appears to improve the reproducability between the preliminary and final results.

The discriminator thresholds should be set dynamically using pulse waveforms identical to those expected since there is some shift in response at the speeds of interest. A barrel type pulse shaping network is available which is used with the DC output of the mercury relay pulse generators for pulse simulation. The test control box provides an oscilloscope monitor point and the desired amplitude is monitored on the CRT while trim resistors are connected.

1570 BOARD TAILORING:

The buffer amplifiers tailor for less than 1mV error. The test control box is set to "Hold" shich disconnects the output circuitry of the Peak Detectors and the input pins for the Buffers may then be shorted to board ground to provide the zero reference value. Connect the DVM between the Buffer output pin and board ground, then trim as required. Use the schematic and layout drawing to determine circuit points. Verify the trim after installation of the final resistors. Then check the combination of Peak Detector and Buffer Amplifiers for less than 2mV total error output.

The U8 one-shots can be verified by driving one of the D inputs with the normal channel shaped pulse at a level greater than its respective discriminator threshold and observing the corresponding delay and reset timing. Two timing capacitors are provided for at each one-shot and the following criteria should be met:

U8 ONE-SHOT ADJUSTMENT

Pin 13 output: 2.0 to 2.6uSeconds, trim with C3 and C4

Pin 9 output: 6.0 to 8.0uSeconds, trim with C6 and C5

Use of the mercury pulser (60 Hz rep rate) provides plenty of reset time for the one-shots to recover prior to the next pulse. If a different stimulus is used, keep the repetition rate slower than 10kHz.

The tailoring operation is also a good time to verify operation of the logic and its timing as illustrated on the schematic. Verify each of the waveforms illustrated to confirm all the components are correct and the threshold levels of the hold delay networks proper. The timing diagram also shows the approximate amplitudes of the various waveforms which are somewhat critical.

SPECIFICATIONS FOR LECP PULSE HEIGHT ANALYZER

Power	A/D Circuit Standby	A/D Circuit During Conversion	Peak Detector Circuit
+ 12.0 V	1 mA	17 mA	4 mA
8.0	1	4	7
6.0	1	1	13
- 6.0	nil	8	23
- 12.0	2	4	not reqd.

Resolution - 10 bits - 1023 counts full scale

Accuracy:

Digital voltmeter section with multiplexer (both LEPT and LEMPA models):

0.1% or 1 bit from calibration @ 25°C against channel calibration

0.3% max observed absolute deviation between channels at 25°C

0.6% max observed absolute deviation from 25 to -50°C

0.5% max observed deviation for power supply variation of 10%

See Calibration Table and Test Records for additional data.

Range: LEPT Mode - 0 to 2.00 volts

LEMPA Mode - 0 to 8.00 volts

Peak Detector Characteristics:

Offset error less than 20 mV (1%) over the environment.

Transmitted resolution - 8 bits - 0.5% - 8 mV

Maximum droop error for last channel converted (@ 60°C) - 2% - 30 mV
(@ 25°C) <.6% - 12 mV

Error from 10% power supply variation - less than 0.5% - 8 mV max @ 25°C

Clock Frequency (external) - 50 kHz (range of about 45 to 80 kHz acceptable)

Calibration:

LEPT: 3 point calibration @ 0.2%, 6%, and 45%. Counts 0002, 0060, 0457 (1023 FS)

LEMPA: 2 point calibration @ 0.2% and 98.3% Counts 0002, 1005 (1023 FS)

Note the last two bits are not transmitted in LEPT mode and the telemetered values read 000, 060, 456 for Full Scale of 255 counts.

Multiplexer protection: 10 kohm input resistor all channels.

Interface protection : Series resistors all input and output lines

Output levels have 100nSec risetimes.
Output levels are 15KΩ to ground when power is OFF.

Calibration Table for Pulse Height Analyzers

		Prototype		Flight One		Flight Two		
		PHA - 1	PHA -2	PHA -1	PHA -2	PHA - 1	PHA -2	
Value of MSB	CH1	1.003	1.002	1.001	1.002	1.003	1.002	Volts
LEPT	Ch2	1.003	1.001	1.003	1.002	1.002	1.002	
Room Temp	Ch3	1.006	1.002	1.004	1.002	1.003	1.003	
	Ch4	1.004	1.003	1.002	1.002	0.995	0.997	
@ -50°C	Ch1	1.002	1.001	0.999	1.007	1.000	1.001	Volts
	Ch2	1.001	1.000	1.000	1.008	1.000	1.002	
	Ch3	1.006	1.001	1.001	1.007	1.000	1.003	
	Ch4	1.003	1.002	0.999	1.007	0.992	0.998	
@ +50°C	Ch1	1.003	1.002	1.003	1.002	1.003	1.001	Volts
	Ch2	1.003	1.002	1.004	1.002	1.003	1.002	
	Ch3	1.006	1.002	1.005	1.002	1.003	1.003	
	Ch4	1.004	1.003	1.004	1.003	0.995	0.998	
Value of MSB	Ch1	4.018	4.010	4.010	4.010	4.003	4.008	Volts
LEMPA - Room T	Ch2	4.015	4.010	4.009	4.008	4.004	4.007	
@ -50°C	Ch1	4.019	4.010	3.993	4.029	4.014	4.005	Volts
	Ch2	4.014	4.004	3.990	4.025	4.007	3.998	
@ +50°C	Ch1	4.019	4.014	4.019	4.013	4.008	4.011	Volts
	Ch2	4.016	4.014	4.019	4.012	4.009	4.010	
LEMPA V offset								
Room Temp		-12	-9	-2	-2	-6	-9	milliVolts
@ -50°C		0	+3	+18	-14	+7	-6	
@ +50°C		-15	-14	-7	-2	-12	-12	
LEPT Cal Reads	0.2%	0002	0002	0002	0002	0002	0002	counts
@ Room Temp	6%	0060	0060	0060	0060	0060	0060	
	45%	0456	0456	0457	0458	0456	0458	
@ -50°C	0.2%	0003	0003	0005	0001	0004	0002	counts
	6%	0061	0061	0063	0058	0062	0060	
	45%	0456	0457	0458	0455	0457	0457	
@ +50°C	0.2%	0001	0001	0002	0002	0002	0002	counts
	6%	0059	0059	0060	0060	0060	0060	
	45%	0456	0456	0458	0457	0456	0458	
LEMPA Cal Reads	0.2%	0002	0002	0002	0002	0002	0002	counts
@ Room Temp	98.3%	1005	1005	1006	1006	1006	1006	
@ -50°C	0.2%	0003	0003	0005	0001	0004	0002	counts
	98.3%	1003	1003	1005	1001	1005	1005	
@ +50°C	0.2%	1001	1001	1001	1002	1002	1002	counts
	98.3%	1005	1006	1005	1006	1006	1006	

REFERENCES

Proposal for Low Energy Charged Particle Measurements in the Jovian, Saturn, and Interplanetary Environments on the MJS 77 Spacecraft - August 1972
T. Krimigis (Principal Investigator)

Technical Description of the Voyager Low Energy Charged Particle Instrument
D. Peletier (Project Engineer) et. al.

Paper: Mariner-Jupiter-Saturn Low Energy Charged Particle Experiment
Peletier, Gary and Hogrefe
1976 Nuclear Science Symposium, New Orleans

Circuit Descriptions and Characteristics of EME Hybrids (all are Test Procedures)

Hybrid No.	Type	Reference
EME-0274A	FET Switch - Type III	LECP-002-75A, 25 July 75, D. Fort
0265A	FET Switch - Type II	as above
0262A	Dual Discriminator	LECP-060-75A, 8 Jan. 76, S.A. Gary
0266	Precision Divider	EME-75-224, 8 Sept. 75, A.F. Hogrefe
0267	Peak Detector	EME-75-186, 5 Aug. 75, A.F. Hogrefe
0268	Unity Gain Buffer	EME-75-193, 12 Aug. 75, A.F. Hogrefe
0269B	Negative Output Op Amp	EME-75-222, 8 Sept. 75, A.F. Hogrefe
0270	Positive Output Op Amp	EME-75-201, 19 Aug. 75, A.F. Hogrefe
0263C	Dual One Shot	LECP-059-75A, 8 Jan. 76, S.A. Gary

APPENDIX A

PHA TEST SET

A special test set is available which allows fast verification of the accuracy and resolution of the PHA in a semi-automated manner. A digital servo loop is used to measure each major bit of the A to D converter. Precision of each bit may readily be observed with a standard digital voltmeter while monotonic progression of the calibration is displayed on an oscilloscope in the region of each major bit. Thereby, one photograph and ten recorded numbers (using a 4 1/2 place or better DVM) completely characterizes the flight hardware for accuracy and resolution. The unit also provides visual decimal readout for all four channels and may be continuously operated at any desired point (using its internal adjustable drive voltage or external precision supplies) for test or trouble-shooting.

The PHA Test Set performs the following functions:

1. Simulates the LECP experiment COMMAND AND DATA ASSEMBLY.
   a) Provides "GO" pulses (variable from about 2 to 40mSec PRP).
   b) Provides "CLOCK" pulses (variable 12 to 27 uSec period).
   c) Has toggle switch control for:

      LEPT/LEMPA select
      D1/D2 select
      CAL/NORM operation
      Power to #1 or #2 PHA.

   d) Accepts PHA outputs:

      DATA
      A
      B
      OUTPUT TIME
      BUSY

2. Converts the binary count out of each of the four PHA time sequenced channels to a BCD signal and displays the resulting decimal number using four LED arrays.

3. Features a digital servo loop to drive an output analog voltage that can be connected to any desired PHA input. This allows:
   a) Automatic lockin to within 1/4 bit of any desired bit for calibration using an external DVM.
   b) Automatic scan of all 10 bits with 1/4 bit dither increments modulating the output analog voltage. Scope horizontal and vertical display drives are available to allow visual analog presentation of the calibration within ± 2 bits of each major

bit. This provides an easy test and photographic record of the most likely points for error in monotonic progression of the scale.

c) Loop may be disabled and its output circuitry used as a precision voltage reference. Helipot panel control allows a range of about zero to 11 volts.

4. Provides oscilloscope monitor outputs for the Data and Timing signals. Generates a Trigger pulse to allow sweep synchronization on the leading edge of the first Output Time interval, thus circumventing the jitter possible due to 1 clock interval uncertainity in PHA initiation ("GO" signal being asynchronous to the clock).

The tester is illustrated by the two block diagrams, Figure A-1, "PHA Test Set Timing and Data Presentation" and Figure A-2, "PHA Test Set Digital Servo Control Loop". The Timing and Data sections of the circuitry can stand alone and may be used to build a PHA readout device if desired. The Digital Servo Control Loop requires inputs from the Timing and Data sections for closed loop operation, but may be used as a simple precision variable power supply in the open loop case. Signals within both sections are made available for DVM and oscilloscope interface. The design is for minimum operator effort during PHA checkout. Schematics and timing diagrams are included herein, for further information contact the author.

APPENDIX B

DISCRETE PARTS LIST

The following list of components shows the approximate number of various components in the discrete section of the electronics for the PHA. The number shown is for one complete flight package. Note there are several special items not found elsewhere in the experiment. These include the reference zener, precision resistors, R/2R ladder network, and one special ± 50 ppm/°C resistor. Also a range of chip values needed for amplifier offset tailoring is shown.

Semiconductors		Number/Package
2N5564	DUAL MATCHED N FETS	2
2N4209	PNP	2
2N2222	AS NPN PAIRS	22
MD-1130	MOTOROLA MATCHED PNP	8
CA-3045	RCA-5 XISTOR ARRAY	2
1N4154	SIGNAL DIODE	6
1N4569A	6.4 V ZENER, MOT., PRECISION	2
HP 2302	H.P. HOT CARRIER DIODE	4
CD 4011	QUAD DUAL NAND	6
CD 4013	DUAL D FF	20
CD 4017	1 OF 10 COUNTER/SELECTOR	4
CD 4023	3-3 INPUT NAND	2
CD 4025	3-3 INPUT NOR	2
CD 4049	HEX INVERTER	4
CD 4050	HEX BUFFER	8
CD 4051	1 OF 8 MULTIPLEXER	4
CD 4052	DUAL 1 OF 4 MULTIPLEXER	2

RESISTORS

PRECISION, ± 0.25%, TC ≤ 15 ppm/°C (T10), TRW/IRC MAR SERIES

10K Ω	MAR-3	4
20K Ω	MAR-3	4
100K Ω	MAR-3	4
250K Ω	MAR-5	4

VICLAN CHIP - SPECIAL T.C., ±1%, ≤ ±50 ppm/°C

10K Ω	20

VICLAN CHIPS - REGULAR ±5%, ≤ 150 ppm/°C

1.2K	5
1.96K	4
5.10K	20
10K	40
27K	16
200K	4
1 MEG	2

Range of possible tailor values in regular viclan resistors - total of about 20 needed per package PHA:

47K, 100K, 120K, 150K, 130K, 220K, 270K, 390K, 560K,

1.0M, 2.2M, 4.7M, 10M

12 BIT LADDER NETWORK:

MICRO NETWORKS CORP - MN-121
R/2R, R=50K — 2 ea.

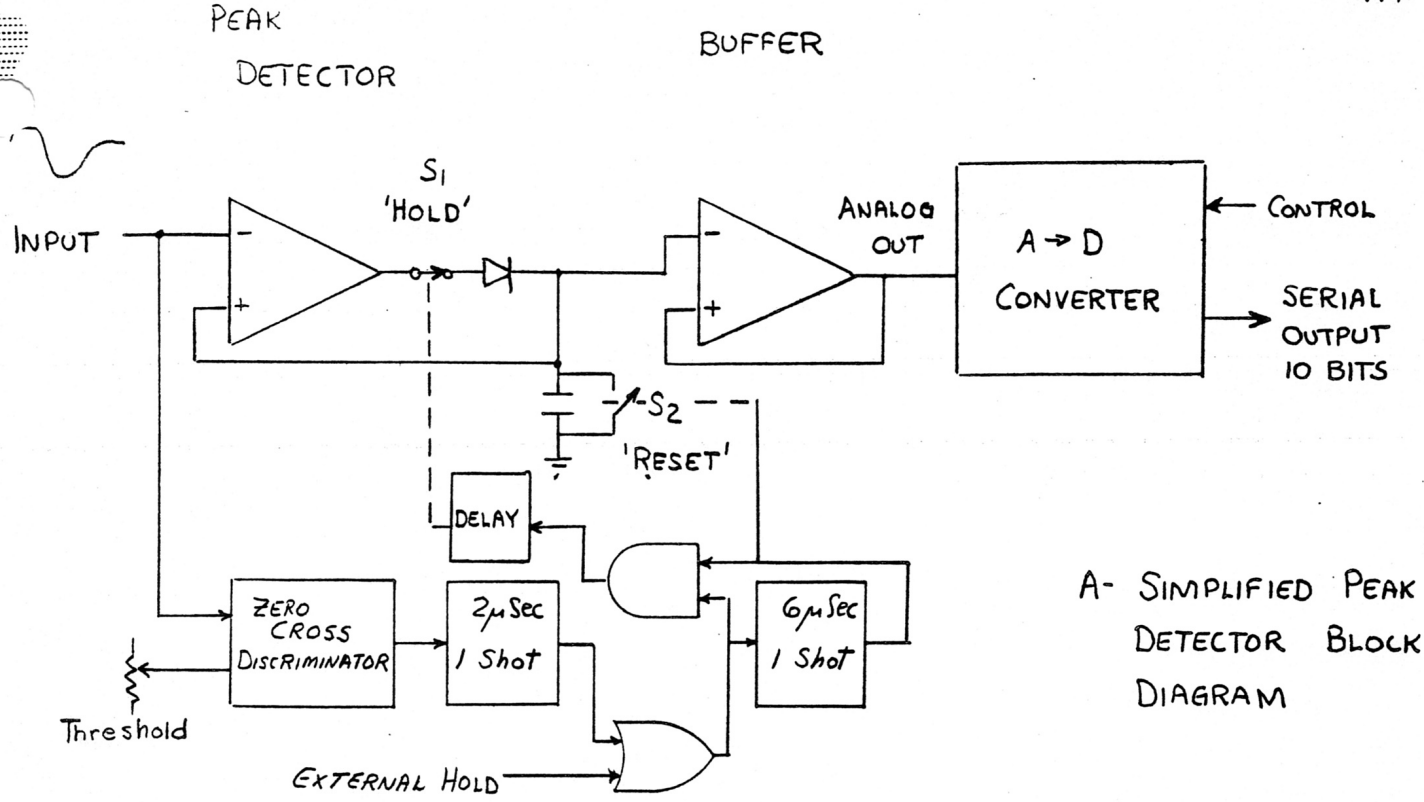
CAPACITORS

22pf	CHIP	10
47pf	CHIP	4
.01μ	CHIP	
220pf	CHIP	2
1.5μf, 15V, ALLOY 182 LEADS, MINITAN		20

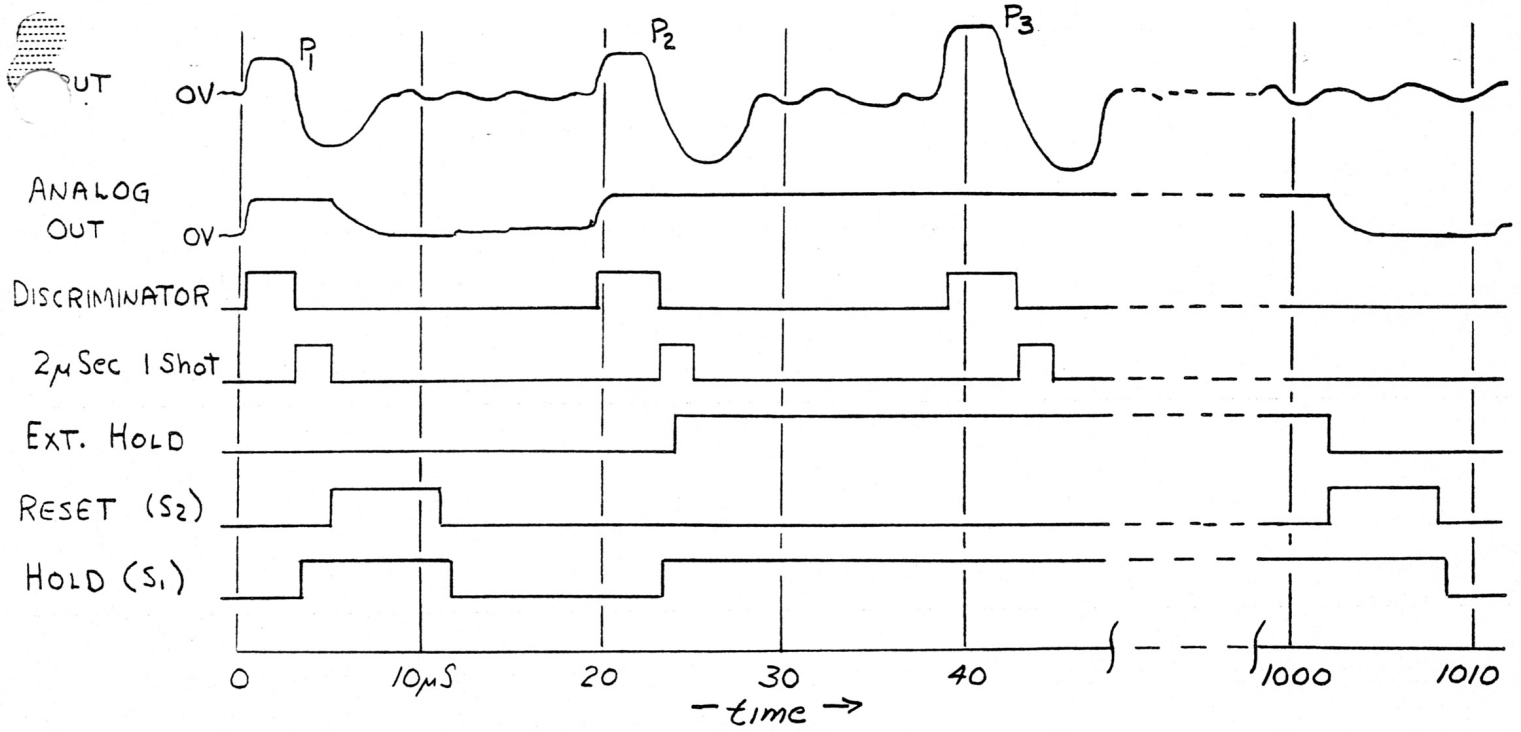
FIG #1 PHA

9 MAR 76

07#



A- SIMPLIFIED PEAK DETECTOR BLOCK DIAGRAM



B- TYPICAL TIMING FOR PEAK PULSE MEASUREMENT

P_1 - NO INTEREST, IMMEDIATE RESET

P_2 - DATA SYSTEM REQUESTS MEASUREMENT

P_3 - GATED OUT (S_1 IS OPEN)

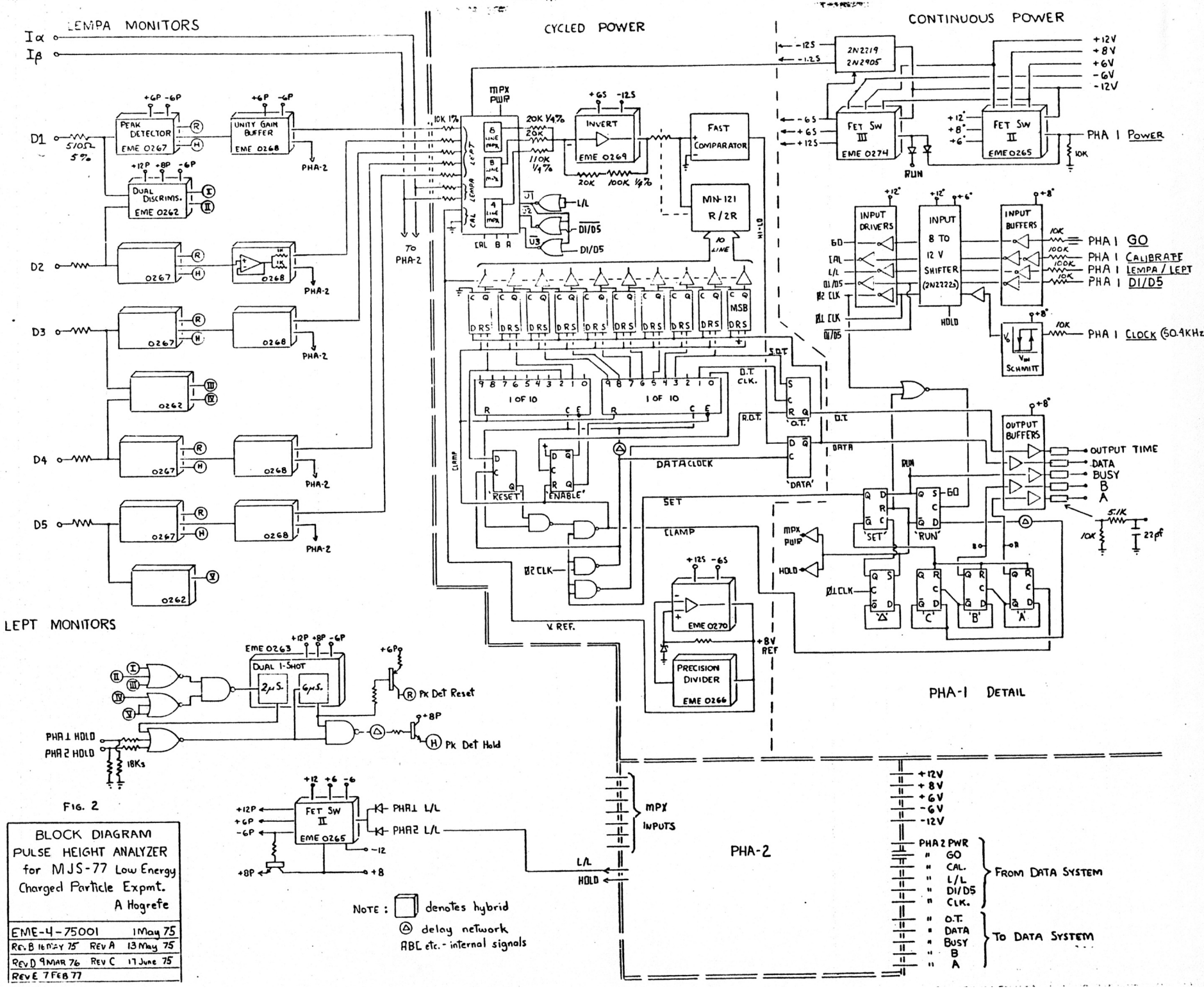


Fig. 2

BLOCK DIAGRAM
PULSE HEIGHT ANALYZER
for MJS-77 Low Energy
Charged Particle Expmt.
A Hogrefe

EME-4-75001	1 May 75
Rev B 16 May 75	Rev A 13 May 75
Rev D 9 MAR 76	Rev C 17 June 75
Rev E 7 FEB 77	

NOTE: ▭ denotes hybrid
△ delay network
ABC etc. - internal signals

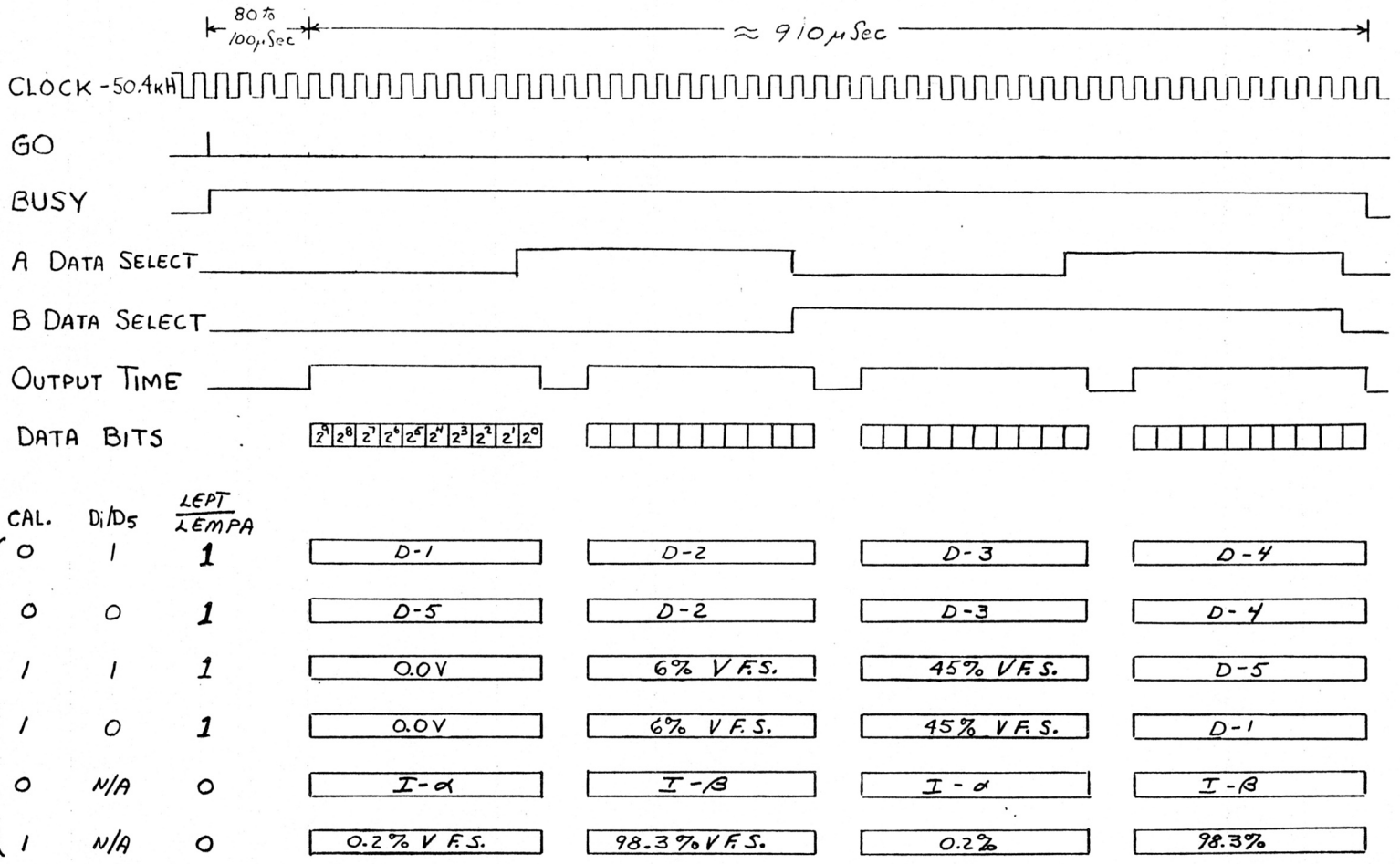


FIG. #3

LECP PULSE HEIGHT ANALYZER
DATA TIMING DIAGRAM

NOTE: TIME FROM 'GO' PULSE UNTIL 1ST DATA BIT IS 4 TO 5 CLOCK PERIODS.

23 OCT 74
07N
REV A 9 MAR 76
REV B 17 DEC 76

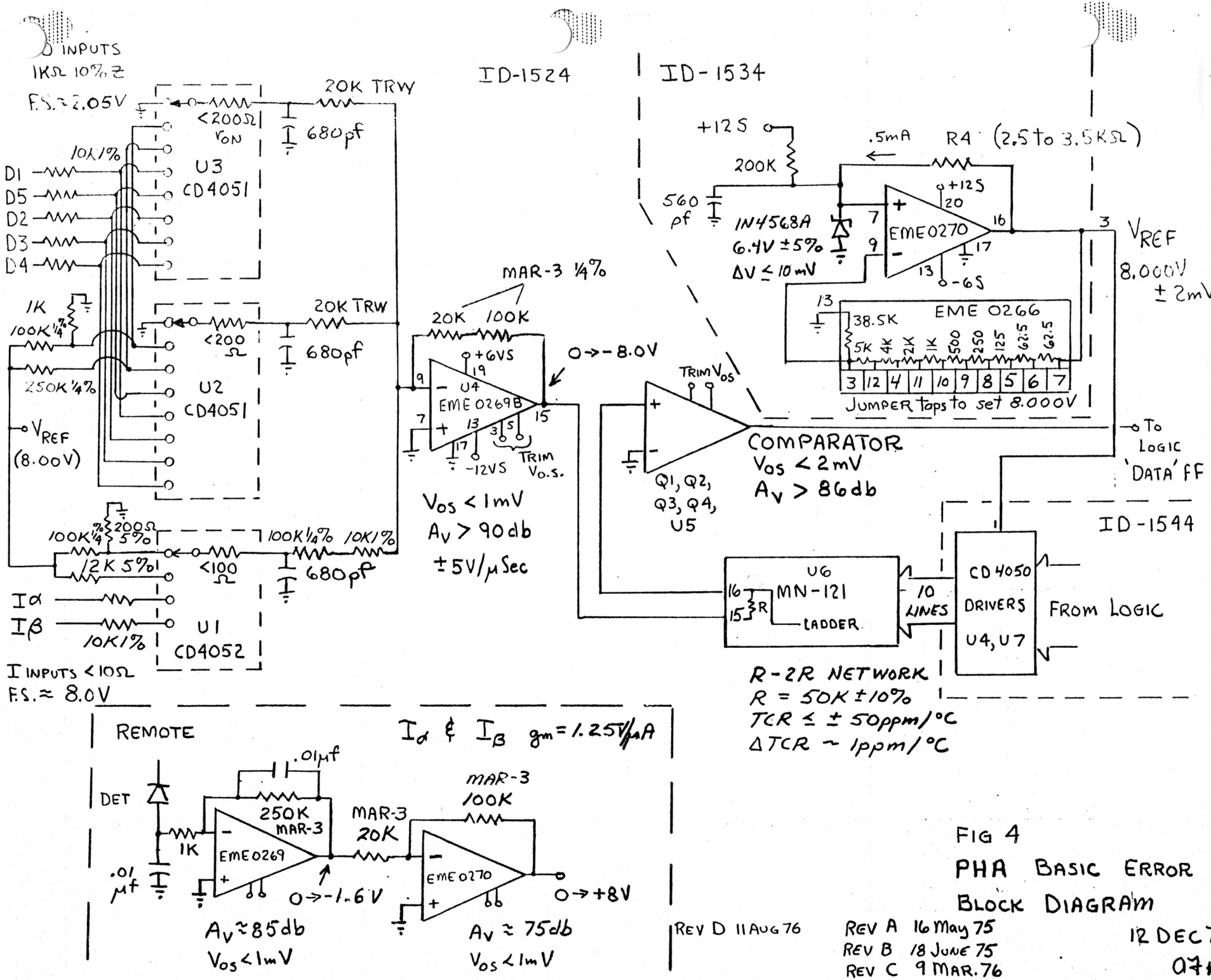


FIG 4

PHA BASIC ERROR BLOCK DIAGRAM

REV A 16 May 75
REV B 18 JUNE 75
REV C 9 MAR. 76
REV D 11 AUG 76

12 DEC 74

07#

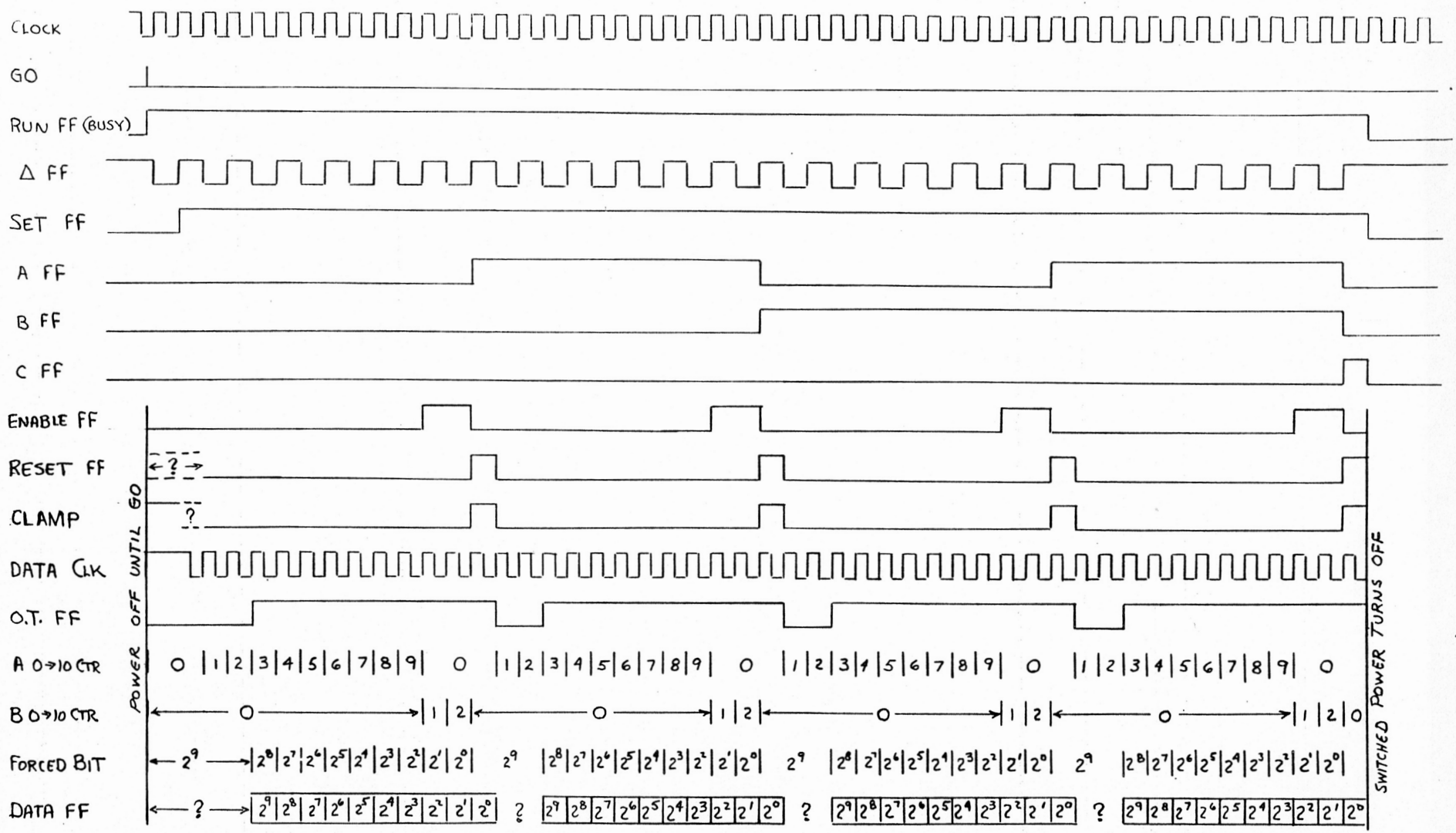
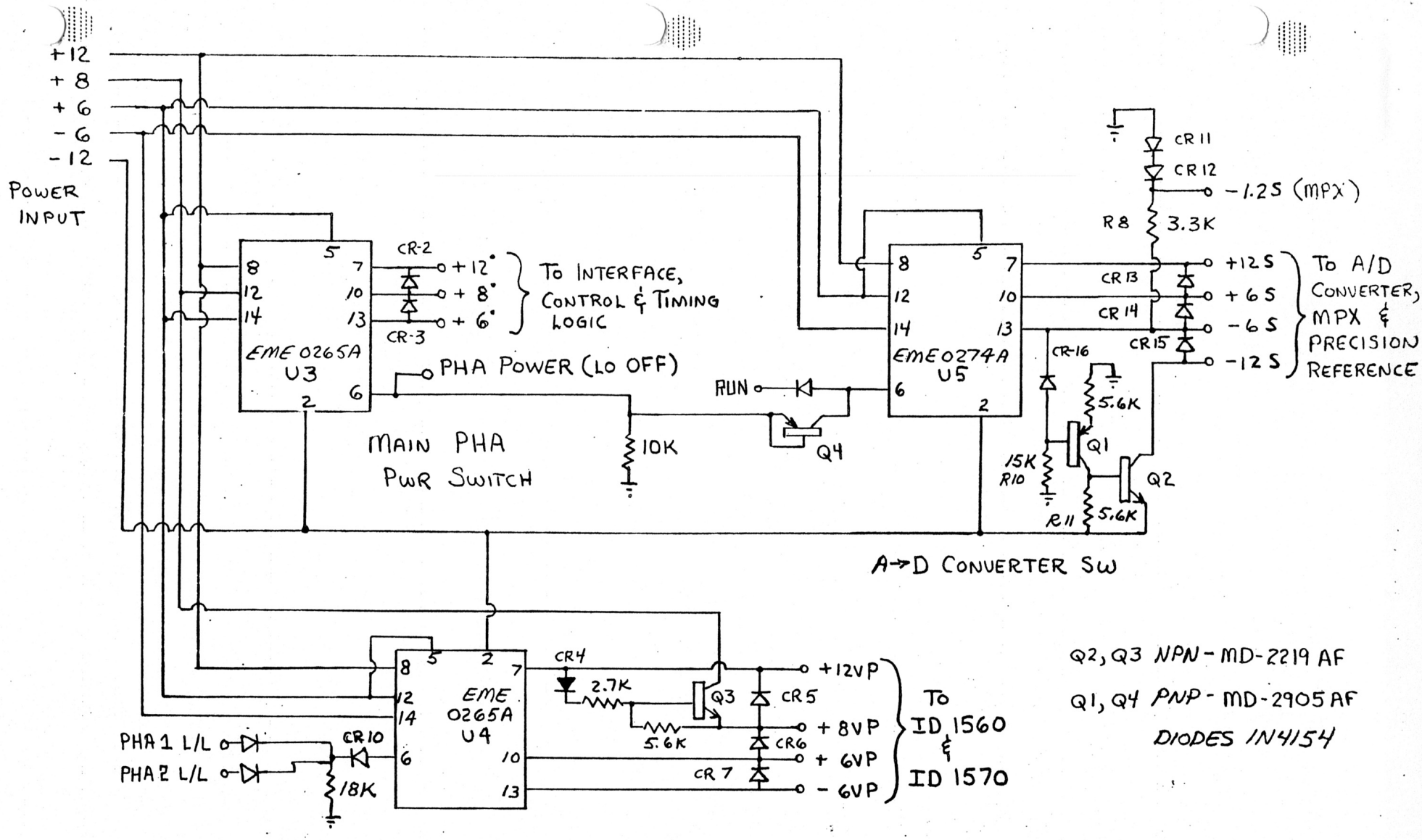


FIG. #5

DETAILED CIRCUIT TIMING
OF LECP PHA A/D CONVERTER
15 MAR 76 GFH



Q2, Q3 NPN - MD-2219 AF

Q1, Q4 PNP - MD-2905 AF

DIODES 1N4154

EME 0265A FET PWR SWITCH TYPE II

EME 0274A FET PWR SWITCH TYPE III

THIS CKT ON ID-1530

2 BDS REQD, PK DET SWITCH (U4 etc.) ON #1 Bd ONLY

FIG. 6

INTERNAL PWR SWITCHES FOR LECP PHA SYSTEM

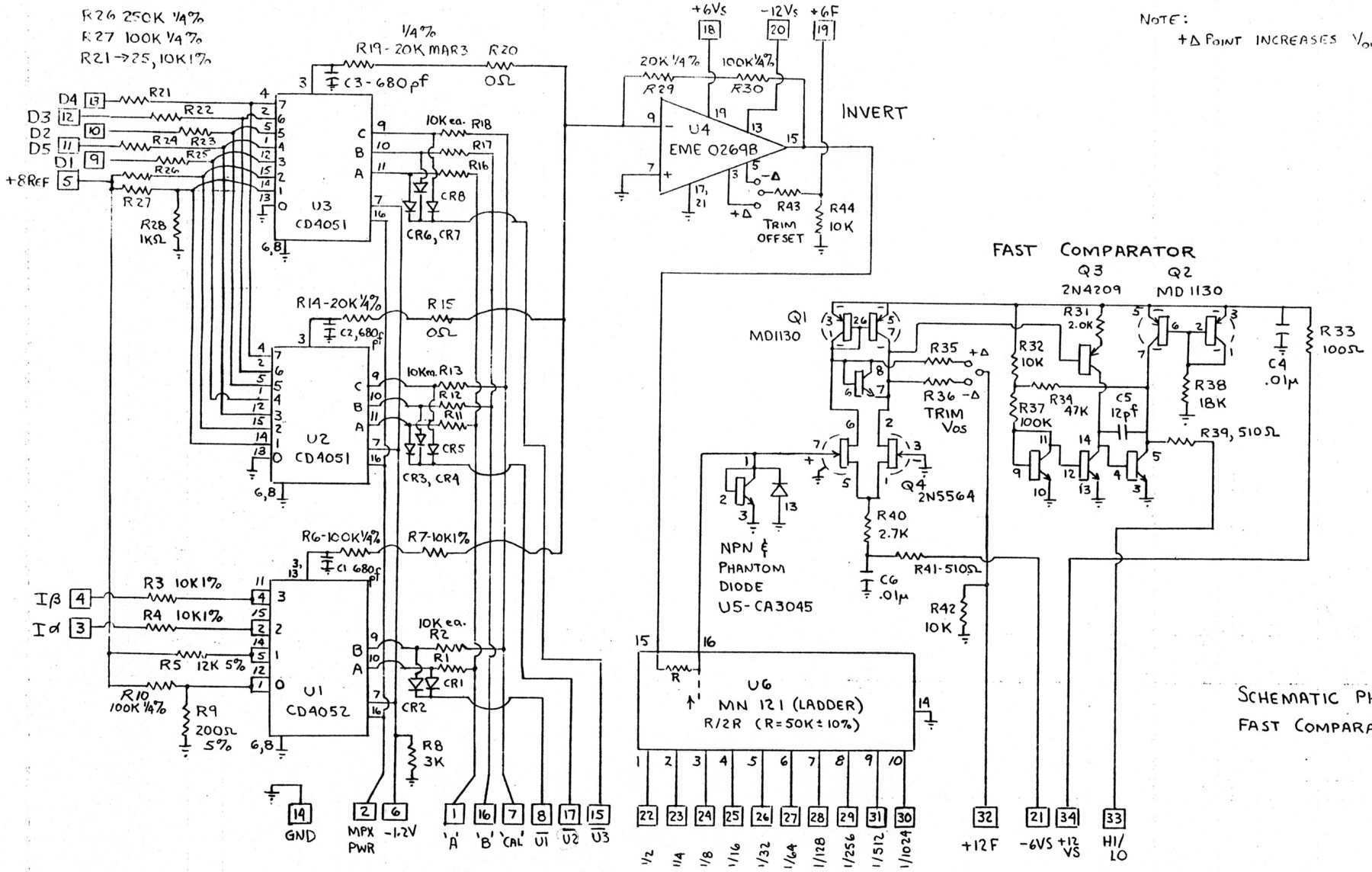
12 MAR 75

07N

REV A 5MAY 75

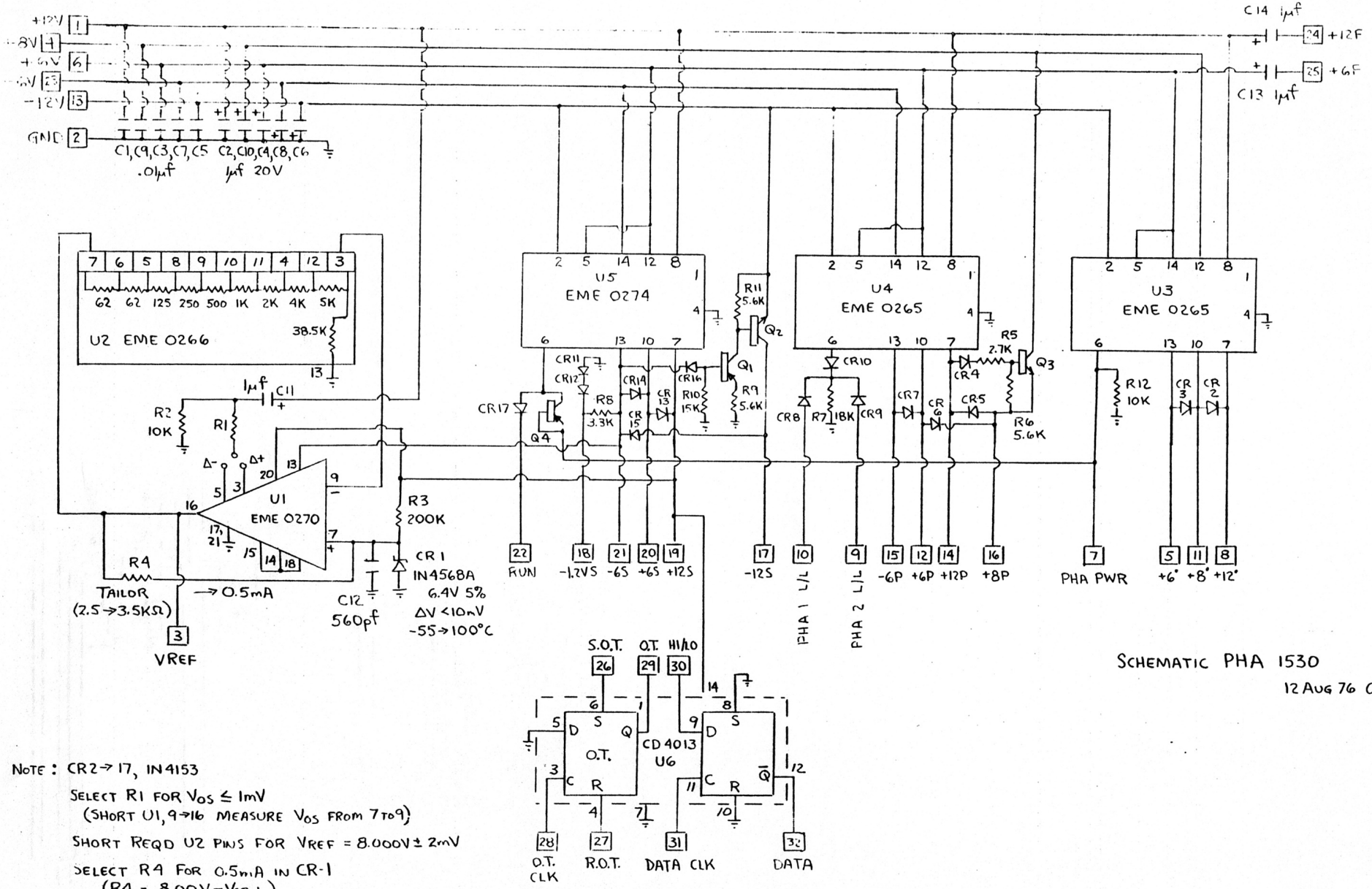
REV B 17JUNE 75

REV C 16 MAR 76



NOTE:
+Δ POINT INCREASES V_{OUT} FOR $V_{IN}=0$

SCHEMATIC PHA 1520
FAST COMPARATOR & MULTIPLEX
11 AUG 76 97H
REV A 21 AUG 76 97H



SCHEMATIC PHA 1530

12 AUG 76 QTH

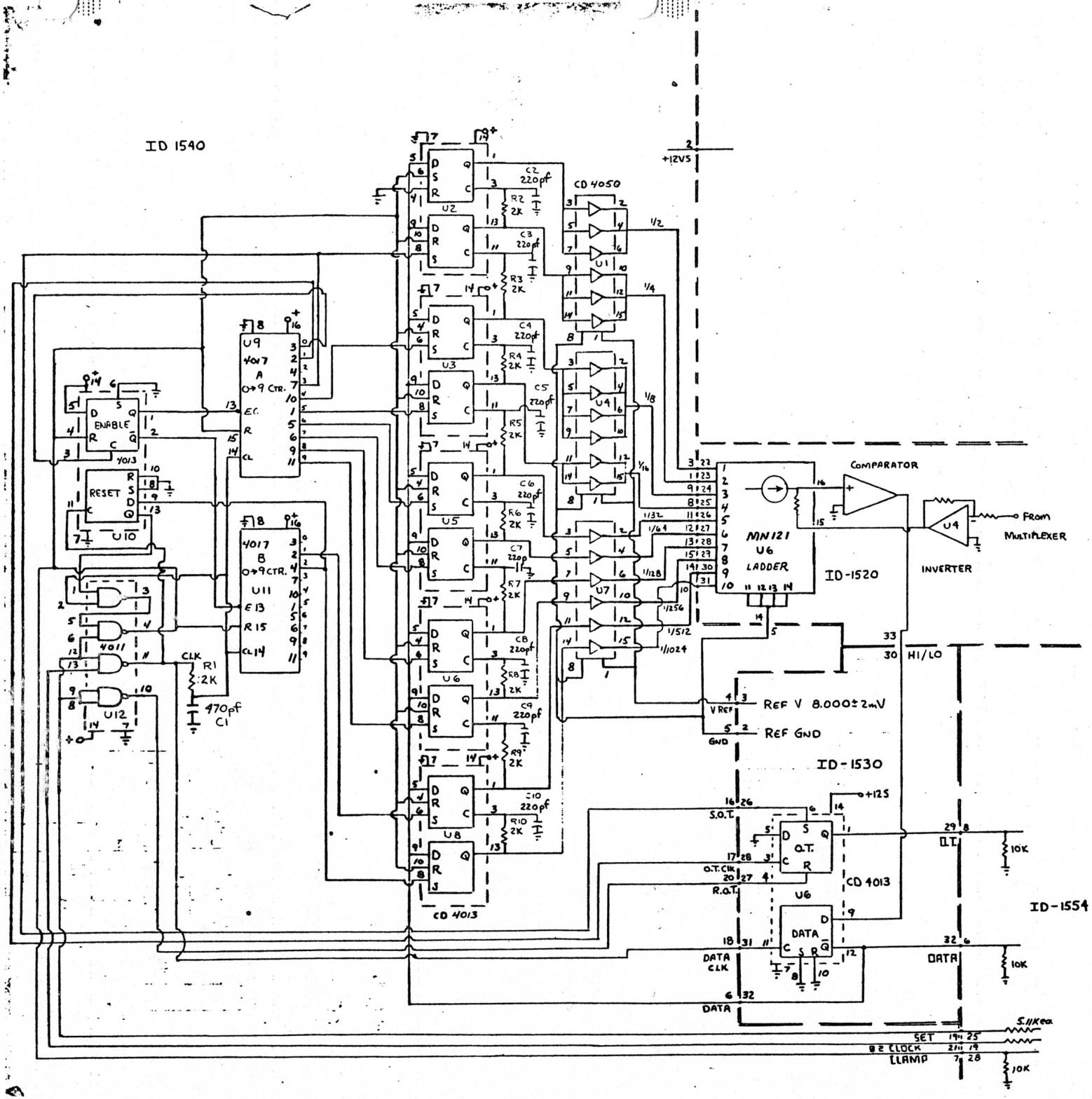
NOTE : CR2→17, IN4153

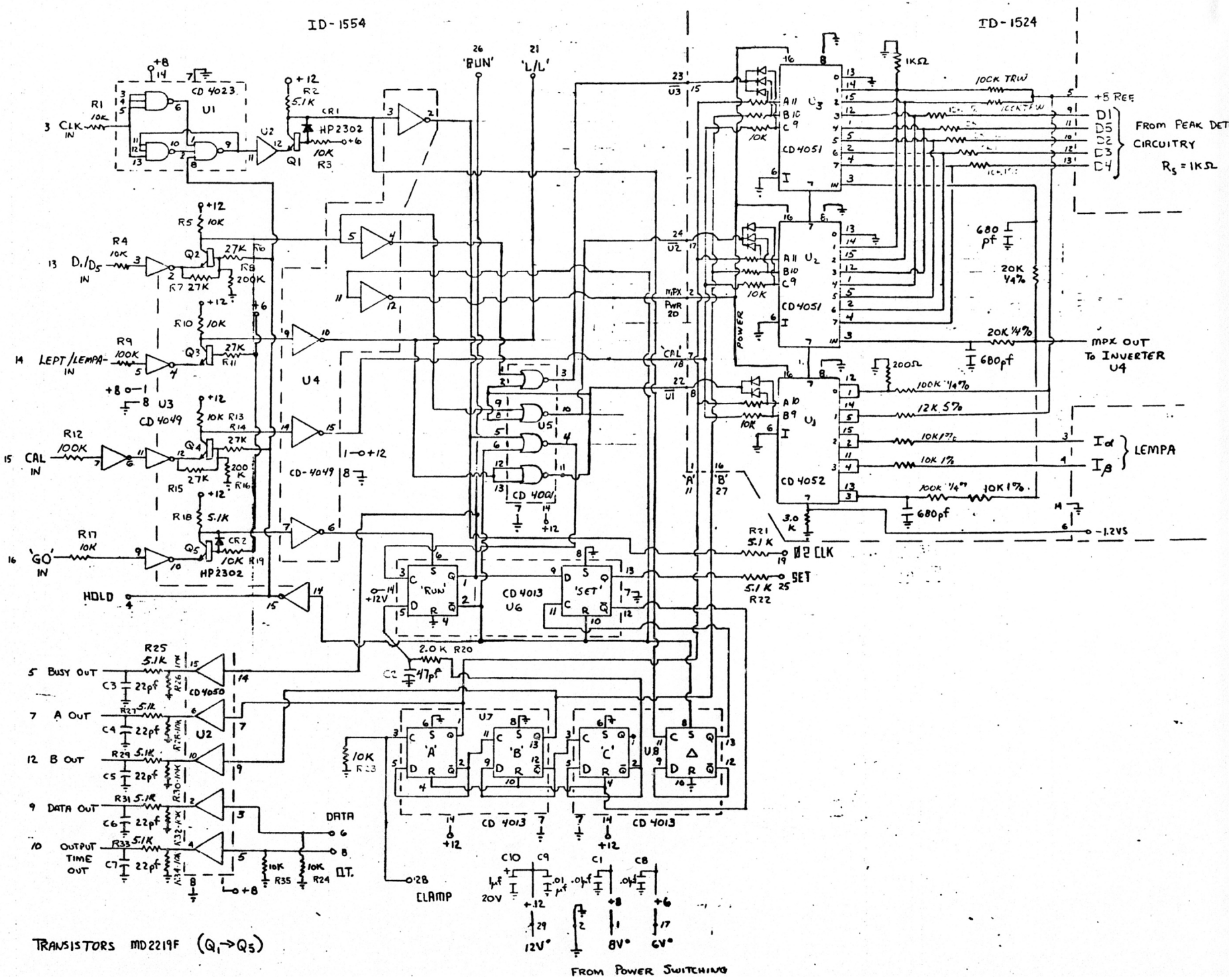
SELECT R1 FOR $V_{OS} \leq 1mV$
(SHORT U1,9→16 MEASURE V_{OS} FROM 7 TO 9)

SHORT REQD U2 PINS FOR $V_{REF} = 8.000V \pm 2mV$

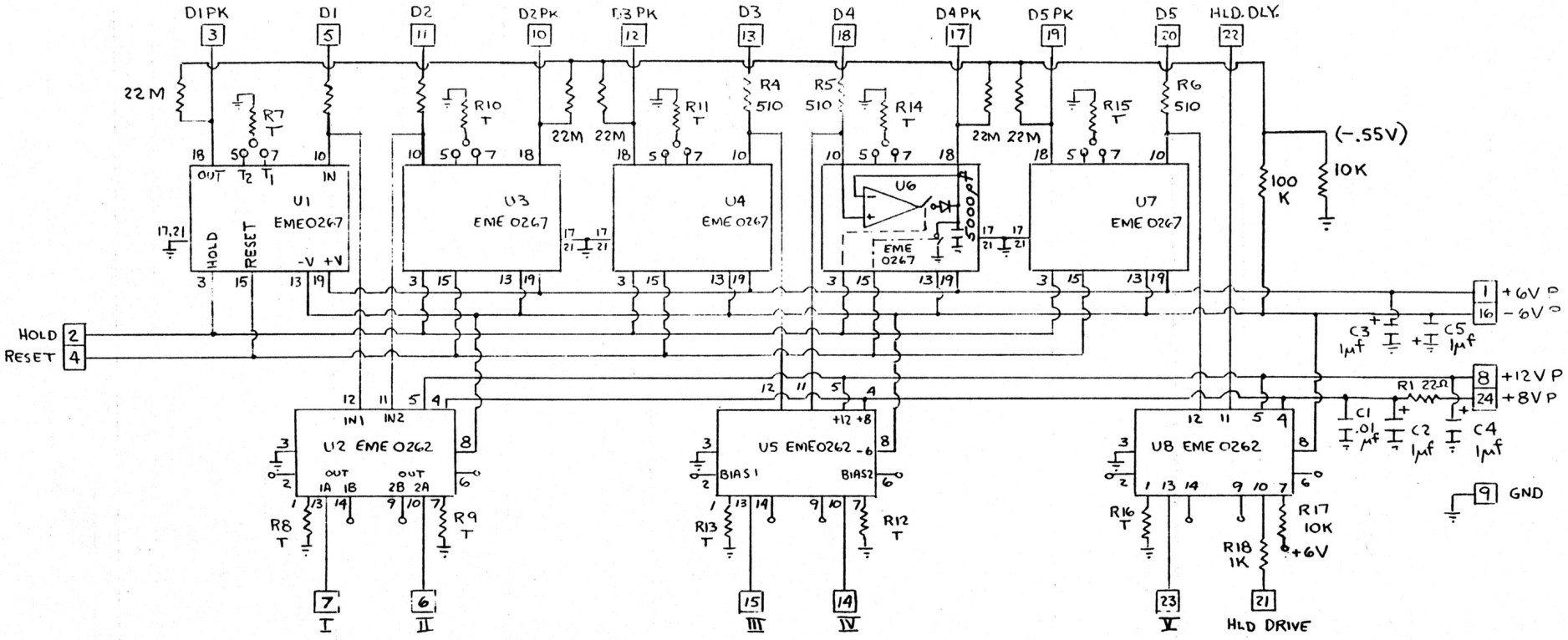
SELECT R4 FOR 0.5mA IN CR-1

$$R4 = \frac{8.00V - V_{CR-1}}{5 \times 10^{-4}}$$


ID 1540
PHA A/D CONVERTER LOGIC
16 MAR 76 G7H
REV A 11 AUG 76
+12V5
CD 4050
U1
U2
U3
U4
U5
U6
U7
U8
C2 220pf
C3 220pf
C4 220pf
C5 220pf
C6 220pf
C7 220p
C8 220pf
C9 220pf
C10 220pf
R2 2K
R3 2K
R4 2K
R5 2K
R6 2K
R7 2K
R8 2K
R9 2K
R10 2K
1/2
1/4
1/8
1/16
1/32
1/64
1/128
1/256
1/512
1/1024
U9
4017 A 0→9 CTR.
U11
4017 B 0→9 CTR.
EN.
R
CL
ENABLE
4013
RESET
U10
4011
U12
CLK
R1 2K
470pf C1
CD 4013
COMPARATOR
MN121 U6 LADDER
ID-1520
INVERTER
From MULTIPLEXER
HI/LO
REF V 8.000±2mV
REF GND
ID-1530
+12S
S.O.T.
O.T.
O.T. CLK
R.O.T.
CD 4013
U6
DATA
DATA CLK
DATA
ID-1554
10K
5.11Kea
SET
82 CLOCK
LLAMP



TRANSISTORS MD2219F ($Q_1 \rightarrow Q_5$)



NOTE:

R7, 10, 11, 14, 15 TAILOR V_{OS}

EME 0262 - DUAL DISCRIMINATORS

SET POS THRESHOLD

$$V_T \approx \frac{R_T \times 8V}{R_T + 62K} \approx 1.3 \cdot 10^{-4} R_T \Big|_{V_T < .5V}$$

$$\& \quad R_T \approx 7.7 \cdot 10^3 V_T$$

DISCRIMINATOR LEVELS

I	410mV	R8
II	330mV	R9
III	100mV	R13
IV	100mV	R12
V	200mV	R16

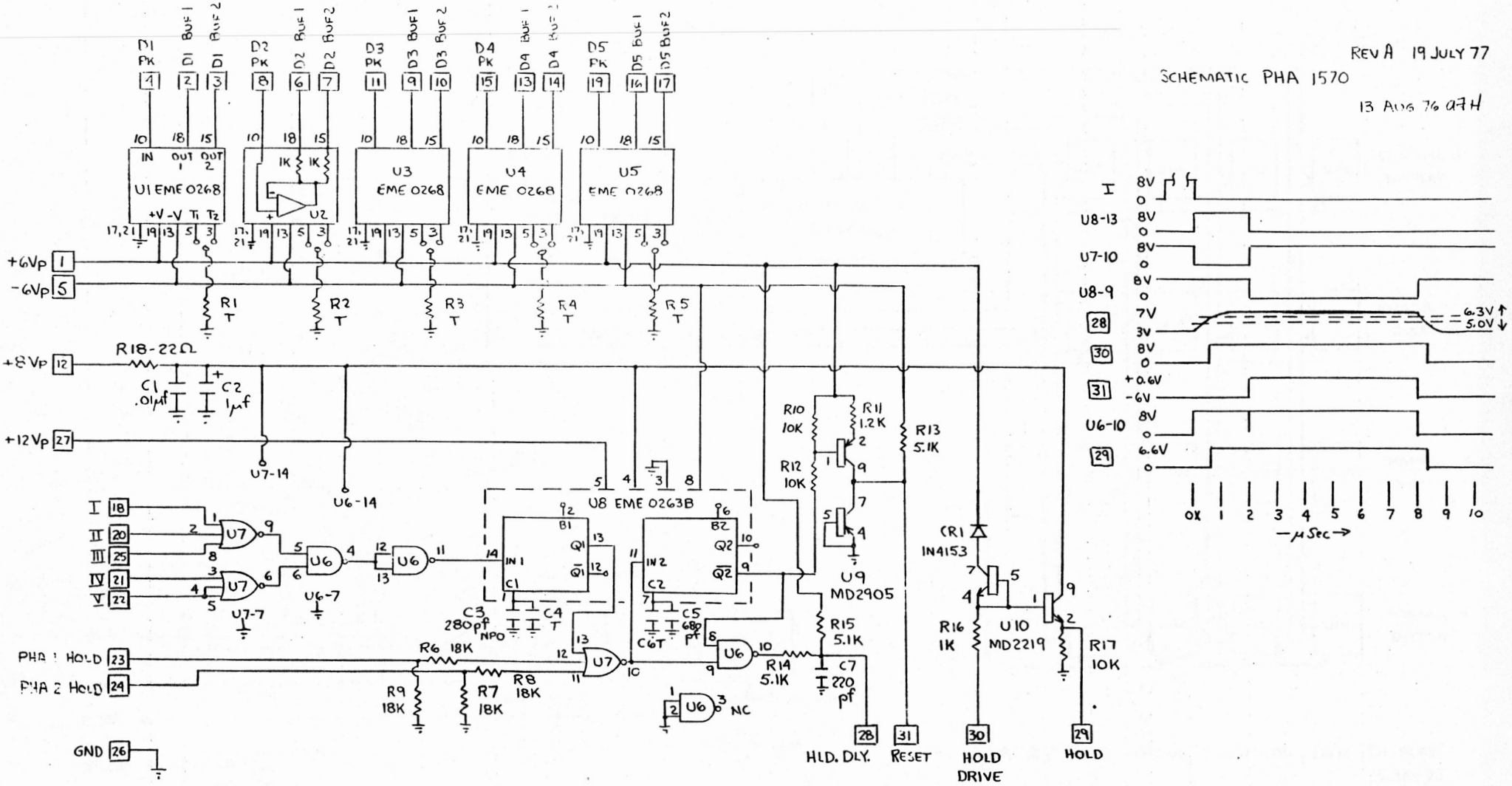
HLD DLY (R17) OUT +8V 0V 5.0V 6.33V IN

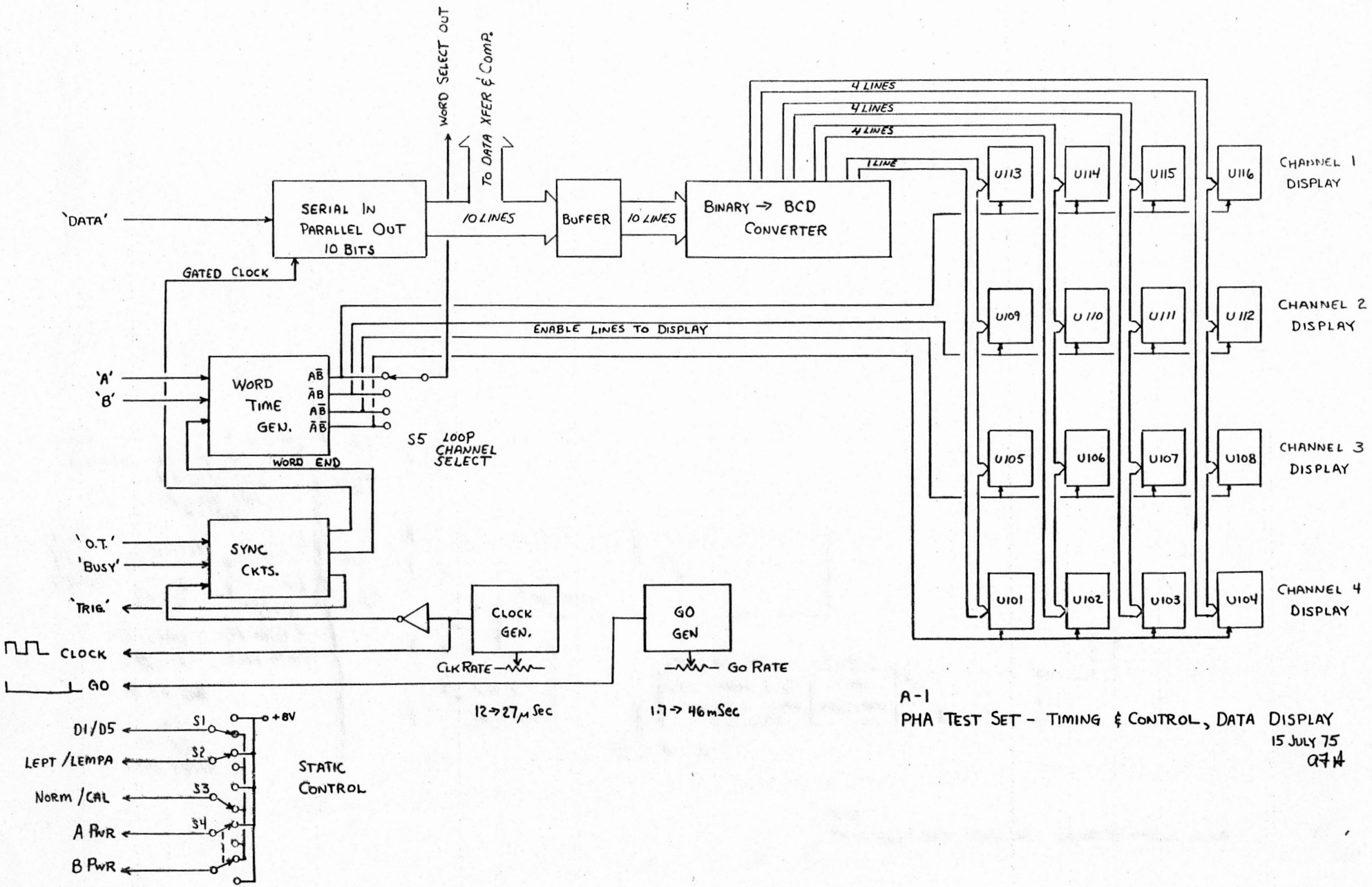
SCHEMATIC PHA 1560
13AUG76 97H
REV A 13 DEC 76 97H
REV B 19 JULY 77 97H

REV A 19 JULY 77

SCHEMATIC PHA 1570

13 AUG 76 07H

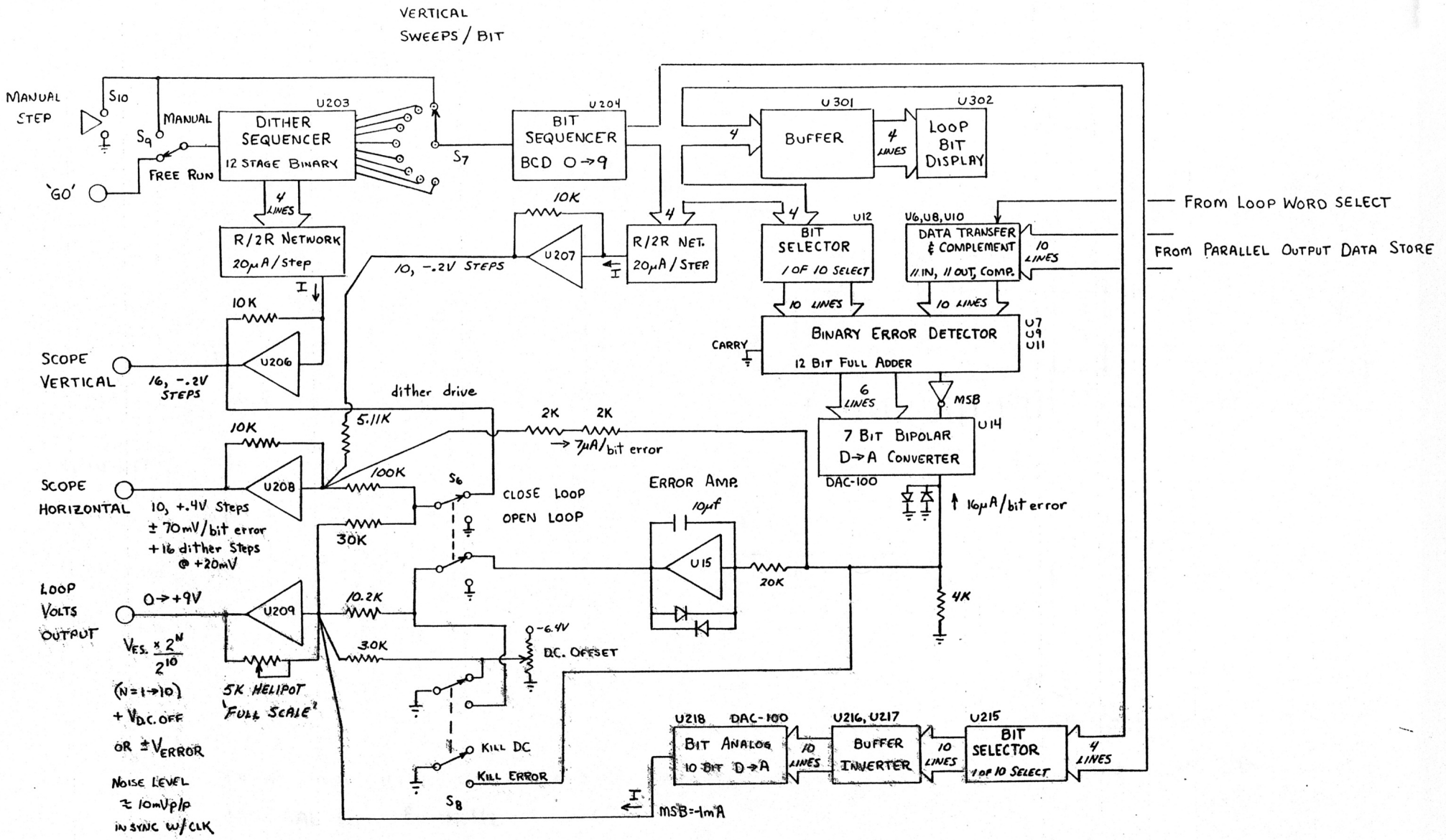




A-1

PHA TEST SET - TIMING & CONTROL, DATA DISPLAY

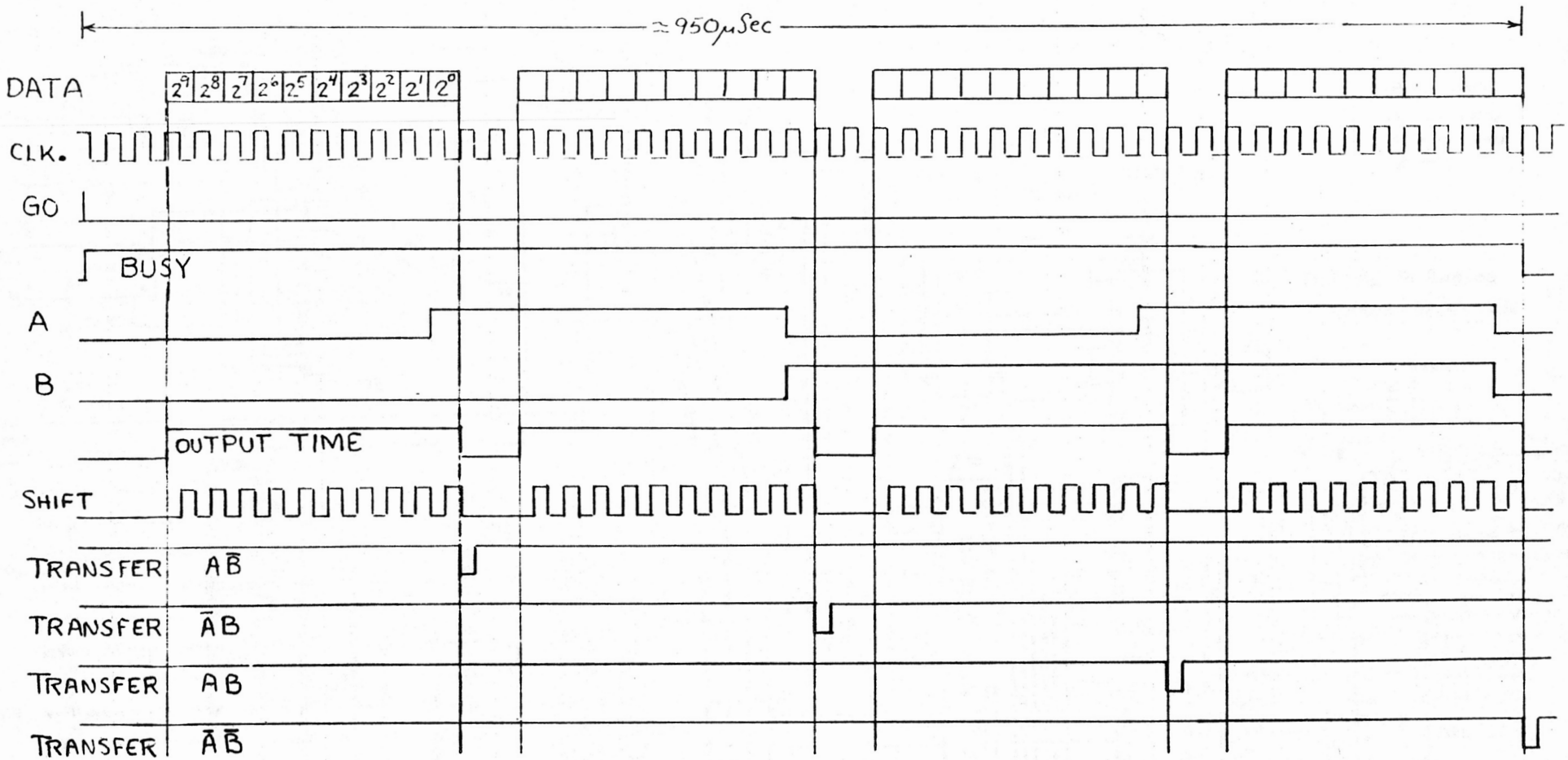
15 JULY 75



A-2
PHA TEST SET - DIGITAL SERVO CONTROL LOOP

7 JULY 75
07H

EME



NOTES:

DELAY FROM 'GO' TO O.T. 2½ TO 3 CLK PERIODS

NOMINAL CLK 50.4kHz

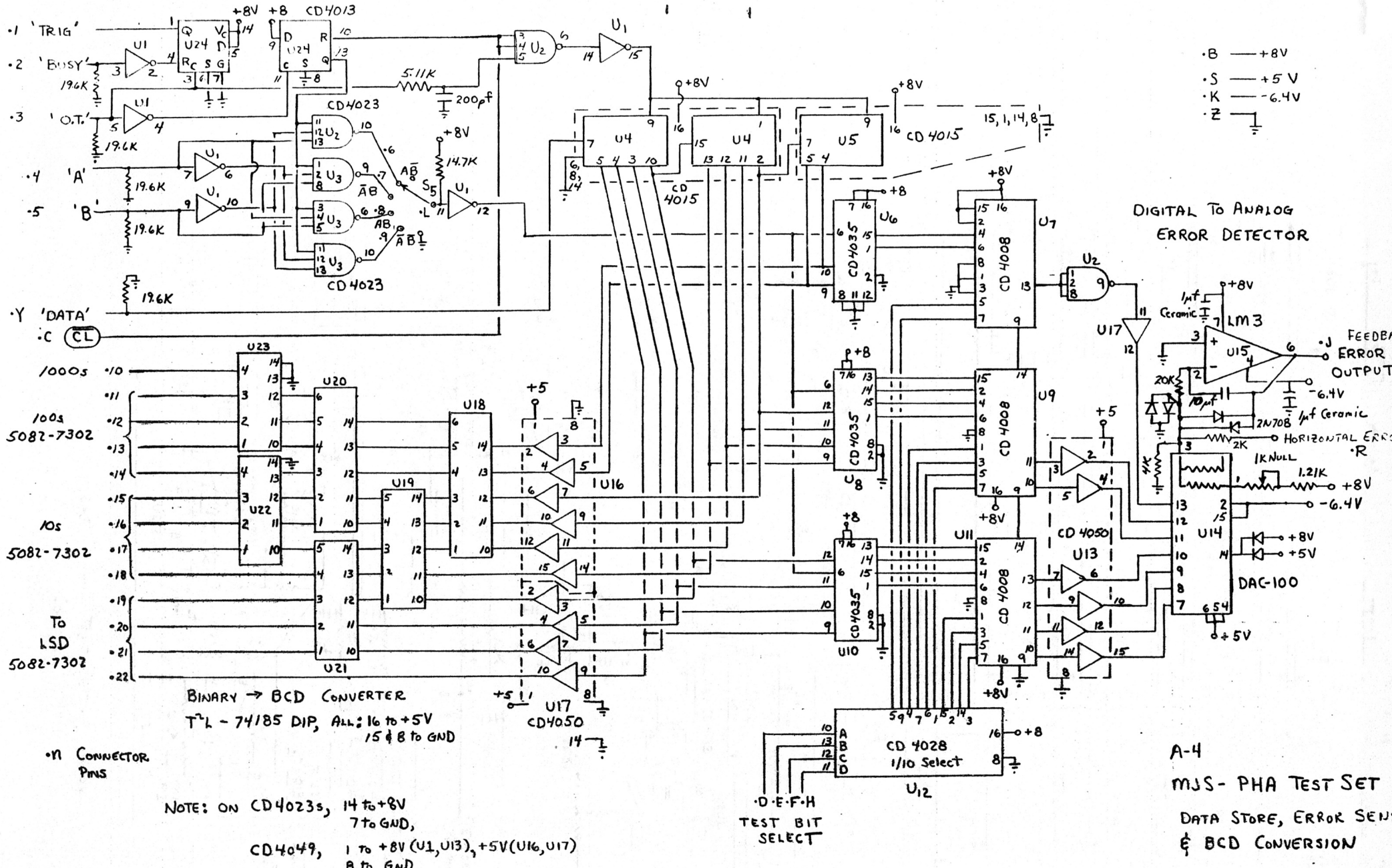
A-3

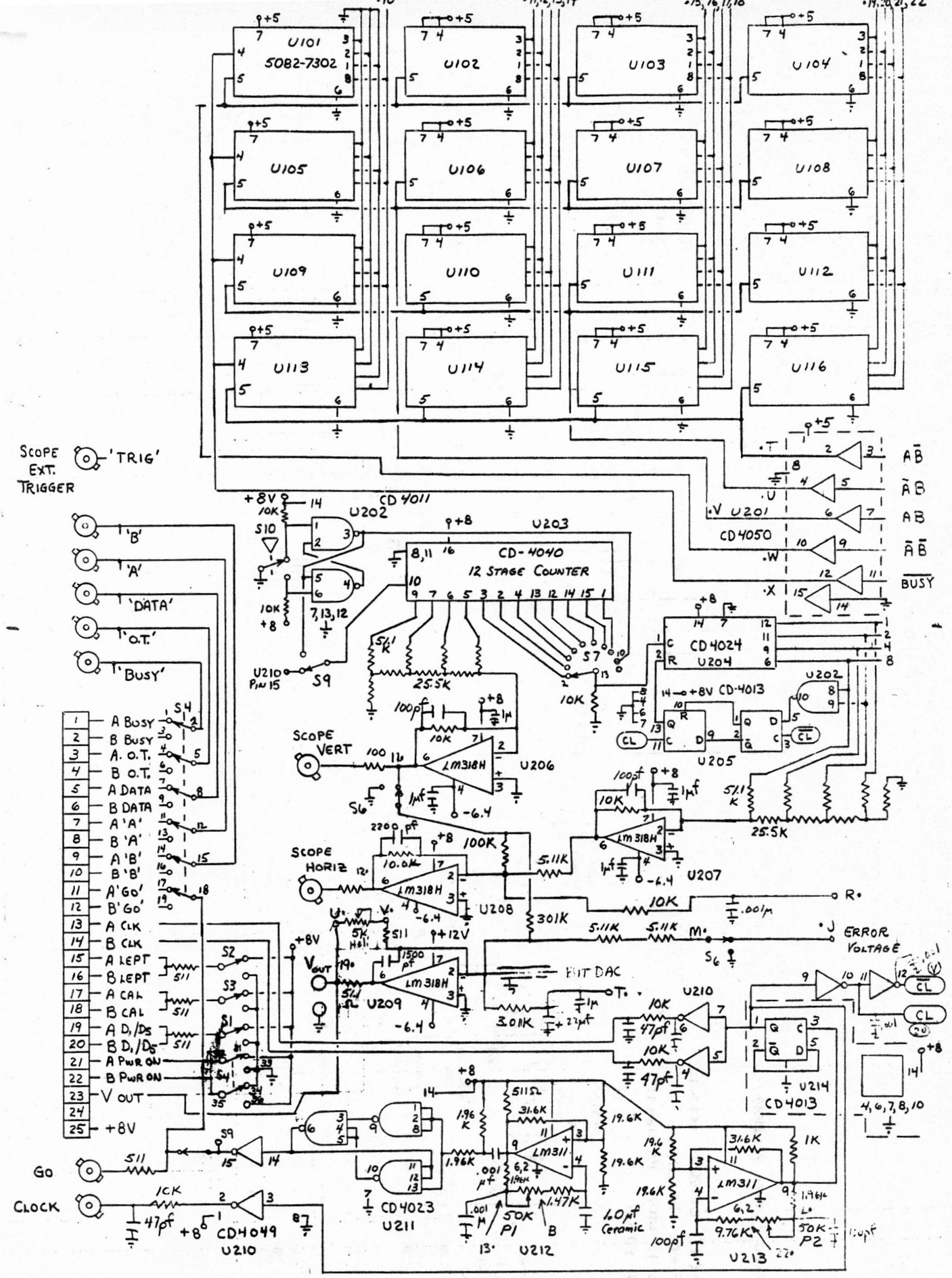
PHA TEST SET

TIMING DIAGRAM

17 JULY 75

CJH

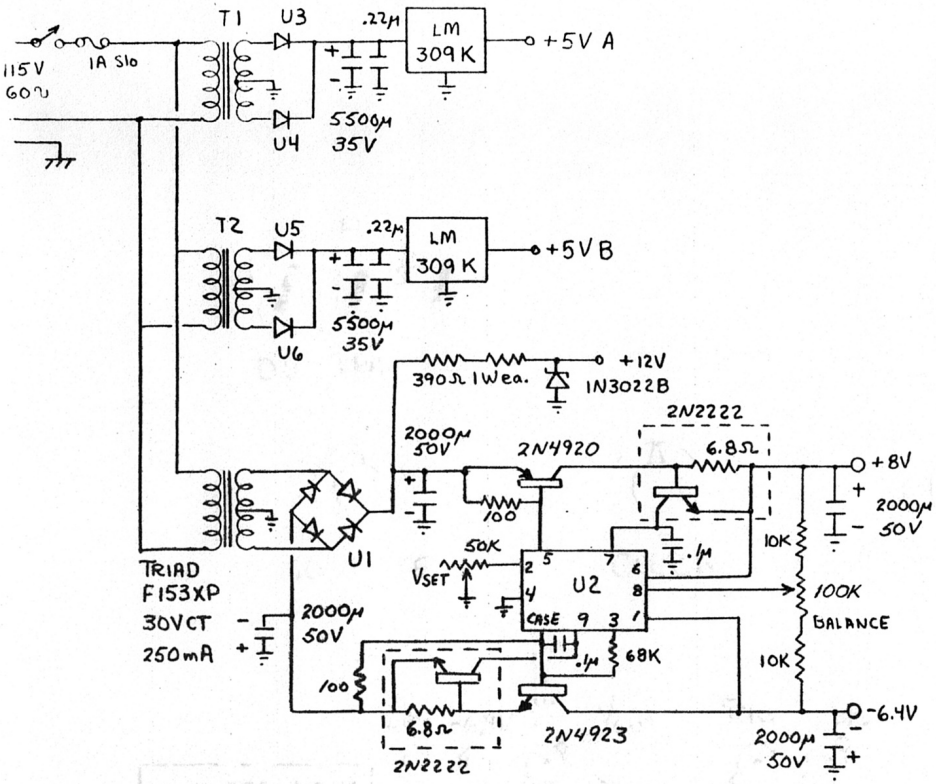

·1 'TRIG'
·2 'BUSY'
·3 'O.T.'
·4 'A'
·5 'B'
·Y 'DATA'
·C CL
·B —— +8V
·S —— +5 V
·K —— -6.4V
·Z
CD4013
CD4023
CD 4015
CD 4008
CD4035
CD 4050
CD 4028
1/10 Select
LM3
DIGITAL TO ANALOG
ERROR DETECTOR
/000s
100s
5082-7302
10s
5082-7302
To
LSD
5082-7302
·10
·11
·12
·13
·14
·15
·16
·17
·18
·19
·20
·21
·22
BINARY → BCD CONVERTER
T²L - 74185 DIP, ALL: 16 to +5V
15 & 8 to GND
·n CONNECTOR
PINS
NOTE: ON CD4023s, 14 to +8V
7 to GND,
CD4049, 1 to +8V (U1, U13), +5V (U16, U17)
8 to GND
TEST BIT
SELECT
·D ·E ·F ·H
·J FEEDBA
ERROR
OUTPUT
·R
HORIZONTAL ERR
DAC-100
A-4
MJS- PHA TEST SET
DATA STORE, ERROR SEN
& BCD CONVERSION
21 FEB 7
07H



A. +8
7 ⏚
17. -6.4V
21. +5V

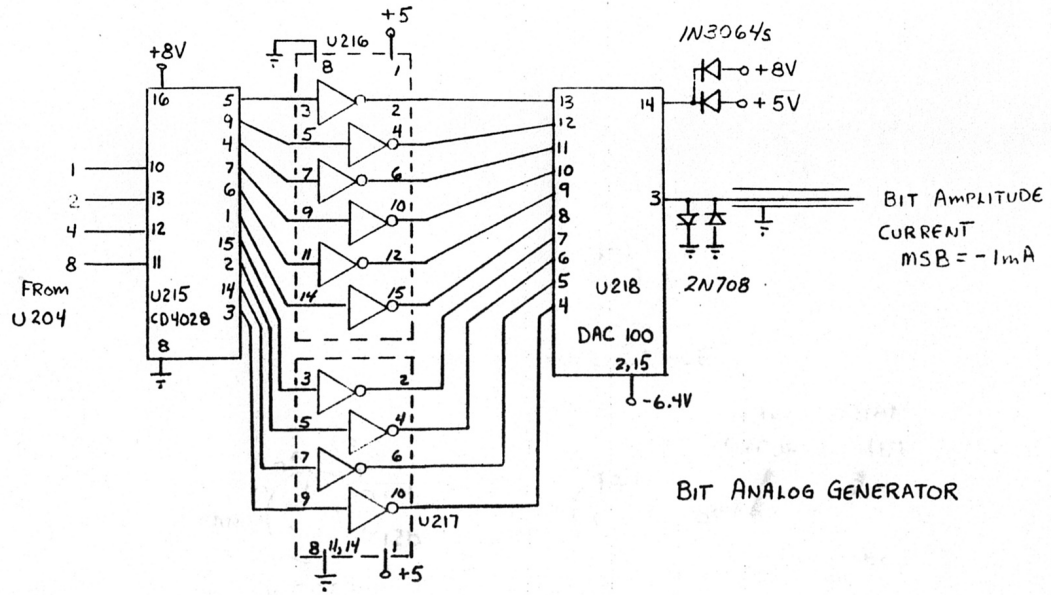
A-5 PHA TEST SET - DISPLAY & CONTROL LOGIC

28 FEB 75

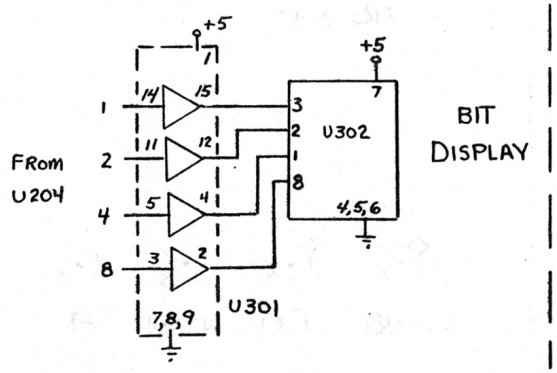


U1 - FD400
U2 - RAYTHEON RC 4194 TK
U3 → U6 - 1N4721
T1 & T2 P8180 25VCT @ 1A

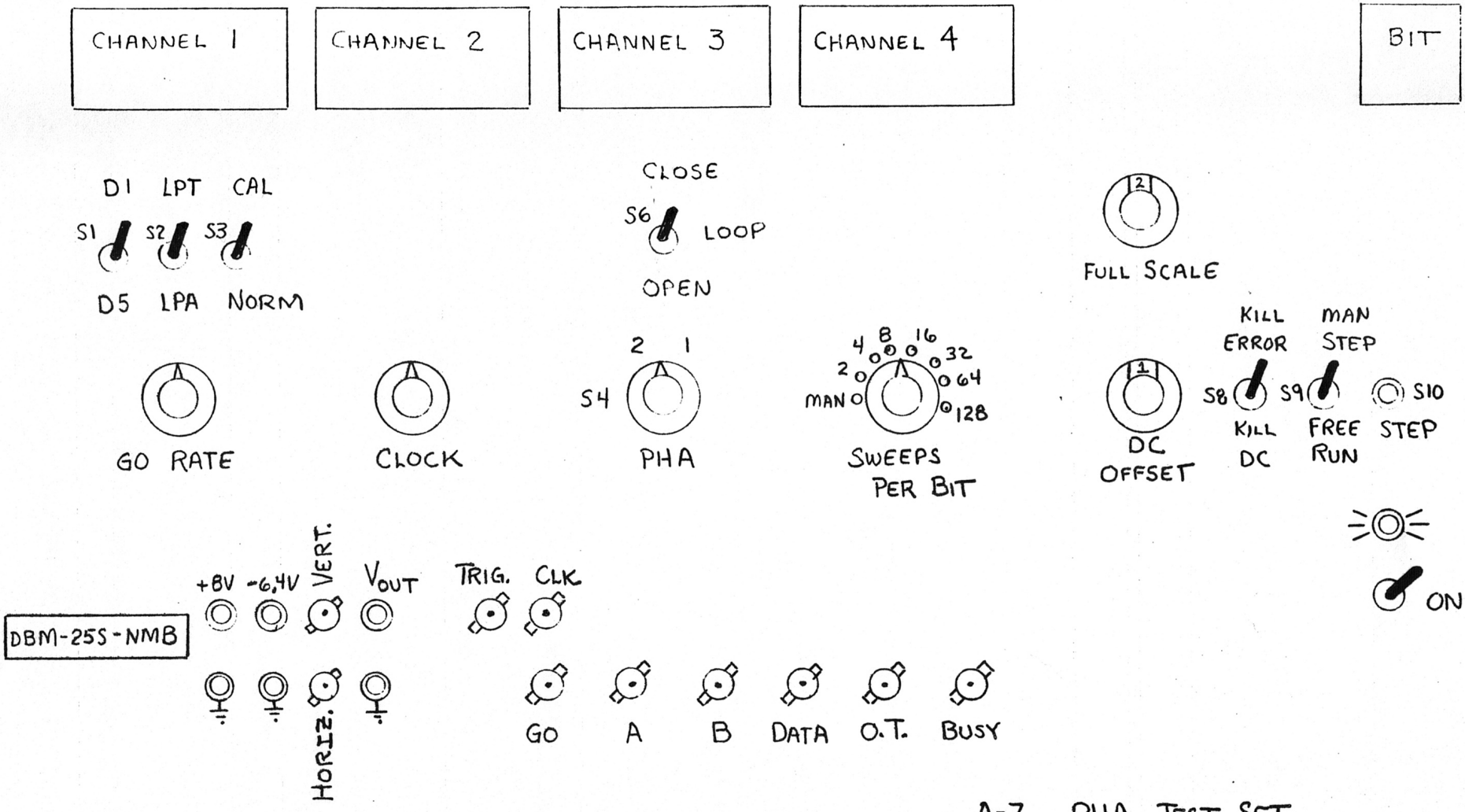
POWER SUPPLY SECTION



BIT ANALOG GENERATOR



A-6
PHA TEST - MISC SCHEMATICS
17 JULY 75



A-7 PHA TEST SET
PANEL DETAIL
18 JULY 75
97A